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Design and Control of Single-Star Bidirectional Boost Modular Multilevel Converter

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Declaration of Authorship

I declare that this thesis titled, "Design and Control of Single-Star Bidirectional Boost Modular Multilevel Converter" and the work presented in it is my own. I confirm that:

- This work was done wholly or mainly while in candidature for a MSc degree at Birzeit University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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المستخلص

تقترح هذه الرسالة قلّاب قدرة متعدد المستويات أحادي النواة مزود من بطارية كهربائية للتحكم بمحركات التيار المتناوب. في هذا التصميم الهيكلي، سيتم توصيل خلايا البطارية مباشرة بقلّاب ثنائي الاتجاه ، مما يسمح بتعزيز المرونة في تصريف وإعادة الشحن للخلية الواحدة وتقليل عدد الوحدات المطلوبة لتشغيل محرك الجر. يلغي استخدام هذا المحول الحاجة إلى نظام إدارة البطارية التقليدي حيث يتم استبداله بالتحكم في القلّاب ، والذي يوازن بشكل تلقائي بين جميع الخلايا. سيتم اختبار القلّاب المقترح تحت الحمل الثابت. سوف يدعم هذا التصميم أيضا احتمالية الشحن للبطاريات من شبكة الكهرباء من مصدر ثلاثي الأطوار. سيتم تقييم أداء المحول المقترح من حيث القدرة على استبدال المحولات التقليدية لقيادة محركات التيار المتردد مع تقليل التشوه التوافقي الكلي وانخفاض الفاقد. سيتم تقديم نموذج مبسط لتقدير فاقد القدرة أثناء التوصيل وتغيير الفواصل للقلّاب متعدد المستويات المقترح مع خلايا البطّارية.

سيتم اختبار النموذج المقترح والتحقق من صحته من خلال استخدام برنامج محاكاة لتأكيد جدوى تشغيل القلّاب المقترحة من ملاءمة الاستخدام لمحرك التيار المتردد ، وصحة نموذج الفاقد ، وفعالية عمليات إعادة الشحن.

Abstract

This thesis proposes a Single-Star Modular Multilevel Converter (SS-MMC) with integrated battery cells to drive an AC motor. In this topology, the battery cells will be directly connected to a bidirectional boost converter, allowing the highest flexibility for discharge and recharge of each individual cell and reduce the number of modules required to run the traction motor. The use of this converter eliminates the need for the traditional battery management system (BMS) since it is replaced by the control of the converter, which balances individually all the cells. The proposed converter will be tested under a static load. The topology will also provide the option for stationary recharge of the battery cells from a three phase AC source. The performance of the proposed converter will be assessed in terms of the ability of replacing the conventional inverters to drive AC motors with low total harmonic distortion (THD) and lower losses. A simplified model for estimating conduction and switching losses for the proposed modular multilevel converter with boosted cells will be presented.

The developed model and topology will be tested and validated by simulation using MAT-LAB to confirm the feasibility of the proposed converter in terms of suitability of use in AC drive, validity of the loss model, and effectiveness of recharging operations.

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List of Abbreviations

BEV	**B**attery **E**lectric **V**ehicle
BMS	**B**attery **M**anagement **S**ystem
CD-THIPWM	**C**arrier **D**ispoition **T**hird **H**armonic **I**njected **P**ulse **W**idth **M**odulation
DS-MMC	**D**ouble **S**tar **M**odular **M**ultilevel **C**onverter
EV	**E**lectric **V**ehicle
FB	**F**ull **B**ridge
FSR	**F**ixed **S**hunt **R**esistor
HB	**H**alf **B**ridge
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
MMC	**M**odular **M**ultilevel **C**onverter
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PLL	**P**hase **L**ocked **L**oop
PWM	**P**ulse **W**idth **M**odulation
SM	**S**ub **M**odule
SOC	**S**tate **O**f **C**harge
SPWM	**S**inusiodal **P**ulse **W**idth **M**odulation
SSC	**S**ingle **S**witched **C**apacitor
SS-MMC	**S**ingle **S**tar **M**odular **M**ultilevel **C**onverter
THD	**T**otal **H**armonic **D**istortion

Chapter 1

Introduction

Due to the increase of CO_2 emission and its harmful environmental impacts caused by gasoline and diesel vehicles, and the limitations of the fuel sources, automobile companies tried to find and develop alternatives to combustion engines, this has led to extend researches in order to reach the use of different energy sources and apply them in various areas to reduce pollution with maintaining high efficiency. One of the major solutions is the Fuel Cell Electric Vehicles (FCEV), Plug-in Hybrid Electric Vehicles (PHEV), and Hybrid Electric Vehicles (HEVs), which reduce the fuel dependency, and greenhouse emissions [1–3].

Development of Electric Vehicles (EVs) industry needs improvement in many aspects, such as developing advanced AC motor drives, improving storage systems efficiency and attaining improved converters based on criteria that guarantee reducing system losses. Many researches work on developing and improving the converters used in driving the Electric Vehicles in terms of reducing losses and increasing efficiency, reducing total harmonic distortion (THD), increasing the output voltage level, and improving many other parameters. Such parameters are to be integrated together to assure getting a reliable performance and an efficient operation.

Many types of traction drives have been used to drive the traction motors in EVs. Conventional two-level inverter was the basic converter used by most of automobile manufacturing companies. Although this inverter is easy to implement and control, it has many drawbacks, such as, low efficiency when it operates at a high switching frequency, and high harmonic contents in the output voltage waveforms. Besides, it requires BMS to balance the series connected battery cells on the DC link, and it has a low reliability. To overcome some of these problems, EV companies are trying to replace their two-level inverters with multilevel inverters such as three level inverters. Three-level inverters have lower switching losses at high frequency compared with two-level inverters, a low voltage rating of the switches, a reduced total harmonic distortion (THD). However, three-level inverters have a main drawback of unbalanced DC-link capacitor voltages [4, 5].

Some heavy electric vehicles require a high voltage drive with a low THD of the output

voltage, and a reduced electromagnetic interference EMI. Therefore, multilevel inverters such as cascaded H-bridges inverter, diode-clamped inverter, or flying-capacitors inverter, are needed to provide the high power and high voltage required by a large EV. The quality of the output waveform in the case of two-level inverter is determined by the resolution and switching frequency of the PWM technique used. Multilevel inverters (directly or indirectly) divide the dc link voltage, so that the output voltage of the leg can have more than two discrete levels. In this way, the output quality is improved, because both pulse width modulation and amplitude modulation techniques can be used. The advantages of multilevel converters compared to conventional two-level converters are well-known, such as, increased number of voltage steps, and a reduced harmonic distortion at the output voltage. There is no voltage sharing problems between devices, and the switches have lower dv/dt than that in the two-level drives [6]. However, in multilevel converters, as the number of steps in the output voltage increases, the number of switches increases, which increases also the complexity of the topology's control.

Recently, Modular Multilevel Converters (MMCs) became widely used in high power applications. MMCs have many advantages over other multilevel converter topologies, such as, its modularity and scalability to meet any voltage requirement, lower losses and high efficiency, reduced THD and consequently the size of passive filters components can be reduced, a low dv/dt on devices and good voltage sharing for semiconductors may be achieved [7].

1.1 Problem Statement and Motivations

At present, two-level inverters are used to drive the Battery Electric Vehicles (BEVs). The DC side of the inverter consists of series connected low voltage cells. Since the cells usually have different leakage currents and chemical characteristics, a State of Charge (SOC) imbalance between them will occur when they are charged and discharged several times. The SOC imbalance reduces their lifetime and may damage them. The battery management systems (BMSs) are usually added to the battery pack to balance the cells by transferring the energy from the high SOC cells to the cells with the lowest SOC. However, they increase the size and cost of the EVs and reduce the efficiency of the overall conversion system.

The BMSs are classified into two main types: passive and active as shown in Figure 1.1. The passive BMSs use resistors to absorb the energy from the cells with the highest SOC to balance them with the lower SOC cells. They are easy to implement and cheap. However, the efficiency is low and the time to balance the cells is too long.

The active BMSs use a specific switching technique to transfer the energy from the cells with

the highest SOC to cells with the lowest SOC. They are divided into three types: capacitor based type, inductor based type, and converter based type. The active BMSs provide higher efficiency and shorter balancing time compared with the passive BMSs. However, they are expensive and more complex in terms of design and control. The next chapter provides a review for some BMSs showing their advantages and disadvantages, and the basic principle of operation for each method.

The output waveforms of the two-level inverter have a significant harmonic content. Therefore, filters must be added to extract the fundamental components of the inverter output waveforms. The reliability of the two-level inverter is quite low. If there is any fault in one of the switches, the converter becomes unable to drive the traction motor and the vehicle must stop for repair.

Recent researches have tried to address the problem of having complex BMSs by designing new MMC called Double Star Modular Multilevel Converter (DS-MMC) [9, 10], which eliminates the need for external BMS to balance the cells voltages. However, it has some drawbacks associated with the high conduction losses, a high-frequency pulsed current in each battery cell, and the need for special controllers to balance the converter's legs and arms.

At the end of this thesis, a new conversion system Single Star Modular Multilevel Converter (SS-MMC) will be designed with the capability of driving the traction motor at a high efficiency, balancing the battery cells without the need for external BMS, and trying to overcome the issues appeared in the previous drives systems.

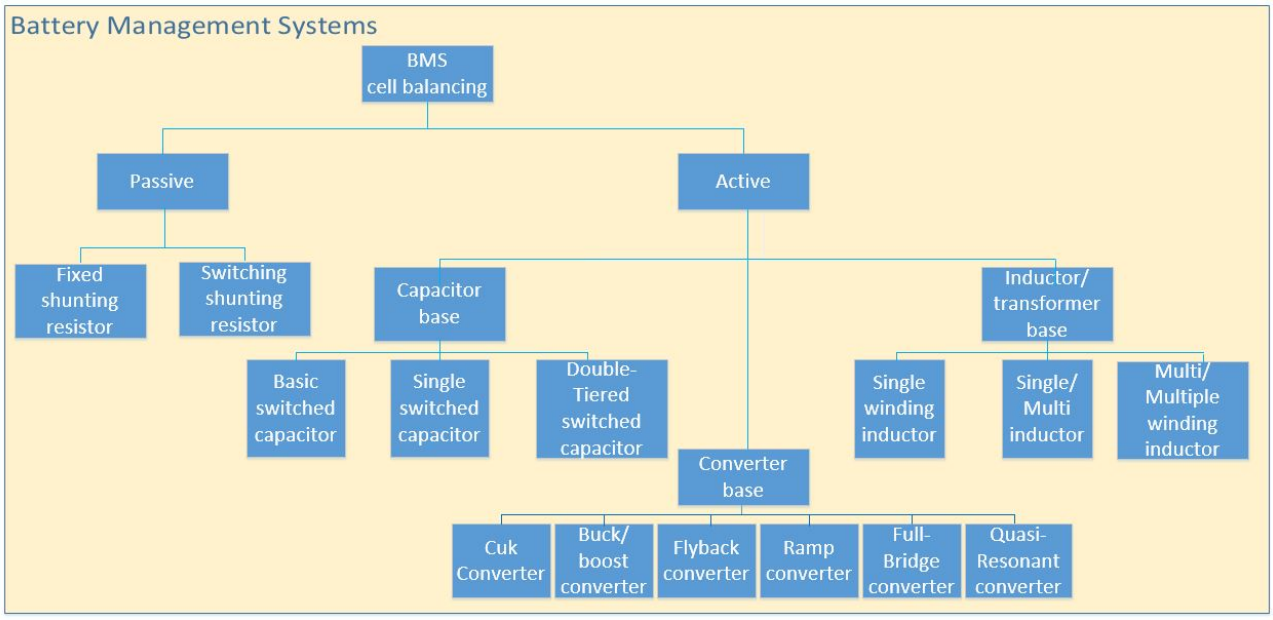

FIGURE 1.1: The diagram of BMSs used in EVs [8]

1.2 Contribution

This thesis proposes some preliminary solutions viewed as contributions in the BEV drives field, for the problems described in section 1.1. Thus, the thesis's contributions are described as follows:

- Bidirectional boost converter will be designed and integrated directly with low voltage battery cells, the boost feature of this converter will help reducing the number of cells required to get a higher output voltage.
- The proposed topology allows the operation with a lower switching frequency, which reduces the switching losses.
- With the use of an appropriate modulation scheme, the converter will be able to develop an output voltage with a low THD.
- The proposed converter is able to balance the battery cells at the same time of energy conversion.

1.3 Research Goals

The objectives of this thesis are as follows:

- To demonstrate the structure and operating principle of the proposed conversion system.
- Develop a comprehensive mathematical model to design the controllers of the overall converter.
- To examine the cell voltage balancing based on applying voltage-balancing algorithm considering the operating conditions with non-equal cell's voltages of the battery.
- To confirm that, the new power converter can be used to drive directly the traction motor from a set of lithium-ion batteries.
- To examine the proposed converter using numerical simulations under static load.

1.4 Thesis Organization

The rest of this thesis is organized as follows:

- Chapter 2 includes a literature review presenting a review for some BMSs used in electric vehicles from different viewpoints and summarizes the advantages and disadvantages for each topology. The rest of the chapter presents a review about the standard EVs drives.
- Chapter 3 introduces the construction and the basic principle of the operation of the proposed converter.
- Chapter 4 presents the simulation results of the system using MATLAB/SIMULINK.
- Chapter 5 includes the conclusion and discussion of the results with possible future work plan.

Chapter 2

Literature Review

The aim of this chapter is to present the methodologies and limitations existing in the related researches conducted in EVs drives. This chapter reviews the main types of BMSs that manage the charging and discharging of rechargeable battery cells in EVs. The chapter also reviews different converters which are used as traction drives.

2.1 Battery Management Systems

Battery Management System (BMS) has an important role in EVs, as it is crucial to protect the battery pack from damage, increase its lifetime, and maintain the battery system in an accurate and reliable operational condition. BMSs are mainly used to eliminate the voltage imbalance between the cells in the battery pack based on their State of Charge (SOC). The Main BMS tasks are summarized as follow [8]:

- Measuring the system voltage, current, temperature, and cells SOC
- Protecting the cells
- Thermal management
- Controlling cells charging and discharging
- Data acquisition
- Monitoring and storing historical data
- Cell balancing

The main issue in battery systems is the imbalance of cells, as it affects battery pack lifetime. cells imbalance comes from two major sources: internal and external sources. The BMSs are classified into two main categories: passive and active as shown in Figure 1.1. The passive

BMSs use mainly passive shunt resistors to remove excess charge from the cells with the highest SOC to balance them with the lowest SOC cells in the battery pack. shunt resistors could be fixed or switched [11–18]. This topology is easy to implement and cheap. However, the efficiency is low and the time to balance the cells is too long.

The active BMSs depends on using a specific switching technique to transfer the excess charge from the cells with the highest SOC to the cells with the lowest SOC. They are divided into three basic types based on the active element used to store energy such as: capacitor based type, inductor based type, and converter based type [8, 11–15, 19]. Active BMSs has advantages over passive BMSs in terms of a higher efficiency and a shorter balancing time. However, they are more expensive, and more complex in terms of design and control.

2.1.1 Passive BMSs

Passive BMSs can be categorized into two sub-categories as was shown in Figure 1.1.

2.1.1.1 Fixed Shunt Resistor

In this method, each cell is connected in parallel with an external resistor as shown in Figure 2.1(a). The resistor value is adjusted to limit the cell's voltage. This topology can only be used for Lead-acid and Nickel batteries as they can be brought into overcharge condition without causing any damage to the cell. This method is easy to implement and cheap. However, the efficiency of this method is low, since it has continuous energy dissipated by the external resistors as heat. A complete balance between battery cells cannot be achieved, since the currents flowing into the external resistors are not controlled [14, 15].

2.1.1.2 Controlled Shunt Resistor

This second method, shown in Figure 2.1(b) differs from the first method, is based on removing the excess energy from the higher SOC cells in a controlled manner using switches or relays. It could work in two modes: a continuous mode, or a detecting mode. In a continuous mode, all switches/relays are controlled simultaneously by the same on/off signal. In a detecting mode, cells voltages must be monitored to detect any imbalance condition to decide which resistor should be shunted. This method is more efficient than the fixed resistor method, simple, reliable, and can be used with Li-Ion batteries [16, 17] .

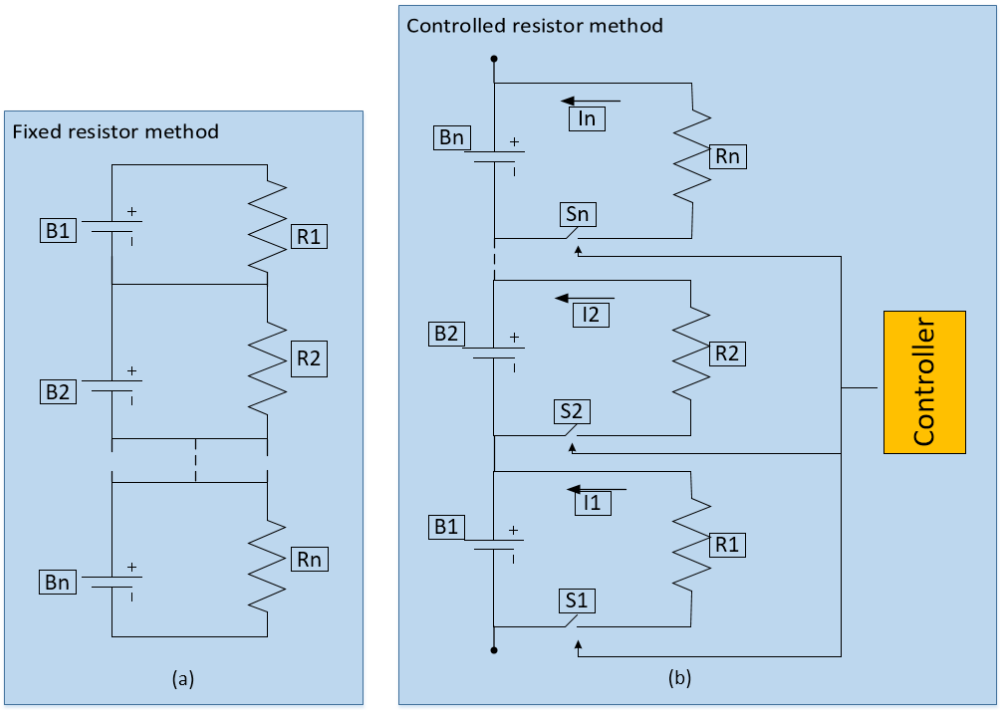

FIGURE 2.1: Passive BMSs: a) Fixed Shunt Resistor b) Controlled Shunt Resistor

2.1.2 Active BMSs

The active balancing method is classified into three main types: capacitor based, Inductor/transformer based, and converter based.

2.1.2.1 Capacitor Based BMSs

It is also known as capacitive shuttling balancing methods. In this type, external energy sources (capacitors) are used to store excess energy to be shunted to battery cells to balance them. This method can be categorized into three topologies as was shown in Figure 1.1: basic switched capacitor, single switched capacitor, and double-tiered capacitor.

1. **Basic Switched Capacitor:** This method is one of the common techniques, which requires '$n-1$' capacitors and '$2n$' switches to balance 'n' cells. The controller of the switches selects the battery cells with higher SOCs and the battery cells with lower SOCs and controls the corresponding switches for shunting energy between them. Figure 2.2 shows the structure of the described topology.

   The main features of this technique are the simplicity of construction and control. However, it has relatively a long equalization time and a low efficiency, since it needs a high number of switches, which will consume a considerable amount of energy as losses [20, 21].

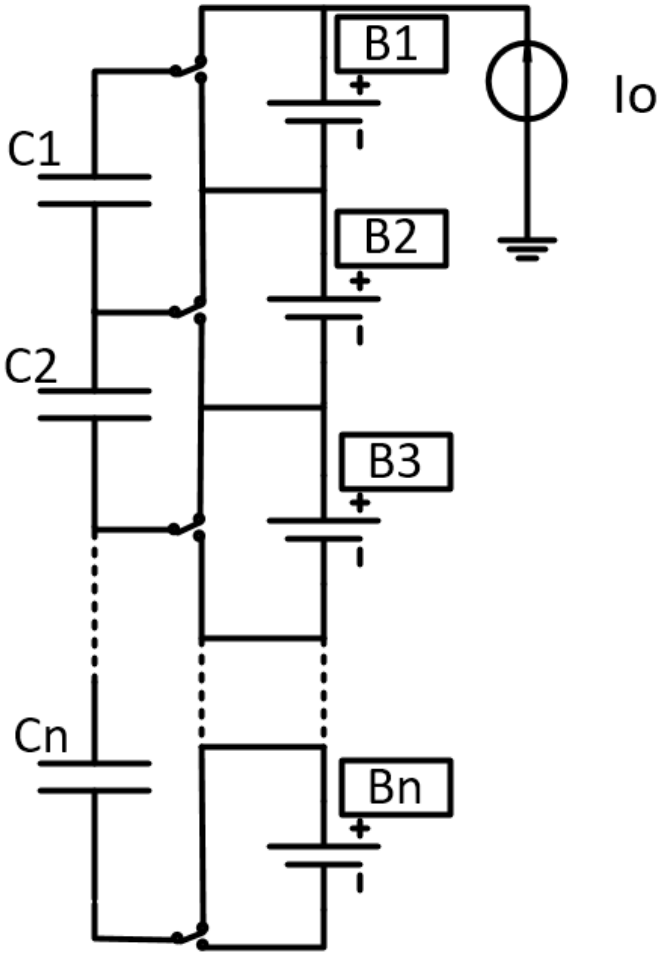

FIGURE 2.2: Basic switched capacitor cell balancing topology [8]

2. **Single Switched Capacitor:** This method is a derivation of the switched capacitor topology as it uses one capacitor with '$n + 5$' switches to balance 'n' cells as shown in Figure 2.3. The higher and lower energy cells with their corresponding switches are selected using a simple control strategy in order to transfer energy between them. An advantage of using this method is that it can work in charging and discharging operation [8, 13, 20] .

3. **Double-Tiered Capacitor:** This topology requires 'n' capacitors with '$2n$' switches to balance 'n' cells as shown in Figure 2.4. it is called double tiered as it has two capacitor tiers for energy balancing. Using this method provides an important advantages over the previous methods, as it reduces the balancing time to quarter. In addition it can work in both operations: charging and discharging [22].

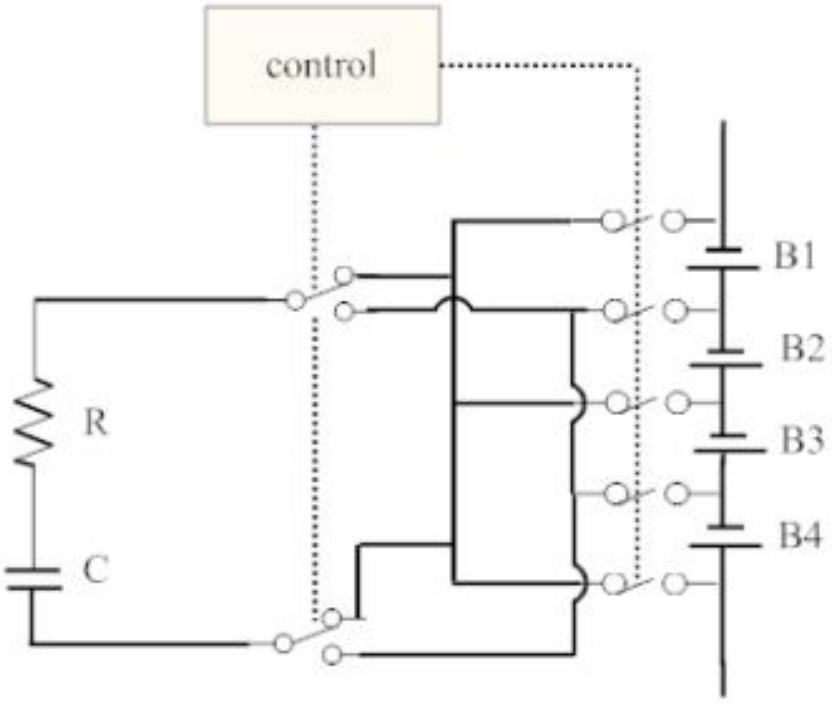

FIGURE 2.3: Single switching capacitor cell balancing topology [8]

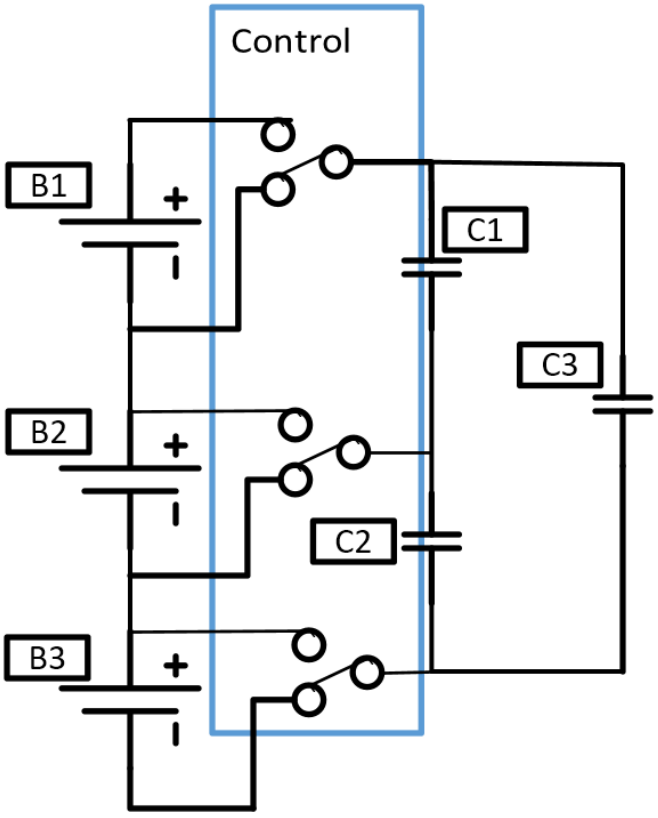

FIGURE 2.4: Double tiered capacitor switching cell balancing topology [8]

2.1.2.2 Inductor/Transformer Base BMSs

In comparison to capacitor base BMSs, this type utilizes an inductor/transformer as the main energy storage element. This category contains three sub-categories based on the type of inductor/transformer used as was shown in Figure 1.1:

1. **Single/Multi-inductor**
2. **Single-Windings Transformer**
3. **Multi-Windings Transformer**

The energy stored in the coils will be used in balancing the cells by transferring energy from the group of cells with a higher SOC to the group of cells with a lower SOC. The main features of this category is that, it offers smaller balancing time whilst maintaining a good efficiency. However, it has some disadvantages such as it requires a complex control system, it has a relatively high cost, and it needs to add filter capacitors across the battery cells in case of using high switching frequency [8, 23].

2.1.2.3 Converter Base BMSs

This method depends on using several types of known electrical converters in balancing batteries as was shown in Figure 1.1:

1. **Cuk Converter**
2. **Buck-Boost Converter**
3. **Flyback Converter**
4. **Ramp Converter**
5. **Full Bridge Converter**
6. **Quasi-Resonant Converter**

One of the main features of these toplogies is that, they have fully control of balancing process. However, they are expensive and complex[8]. In this section, one of the widely used topologies in cell balancing will be discussed, which is the buck-boost converter (BBC) method. Figure 2.5 shows the structure of the balancing system. The converter operates in three modes: buck mode, boost mode, and buck-boost mode. In the boost mode, the excess energy is removed from the higher SOC cell to the DC power source. Whilst in the buck

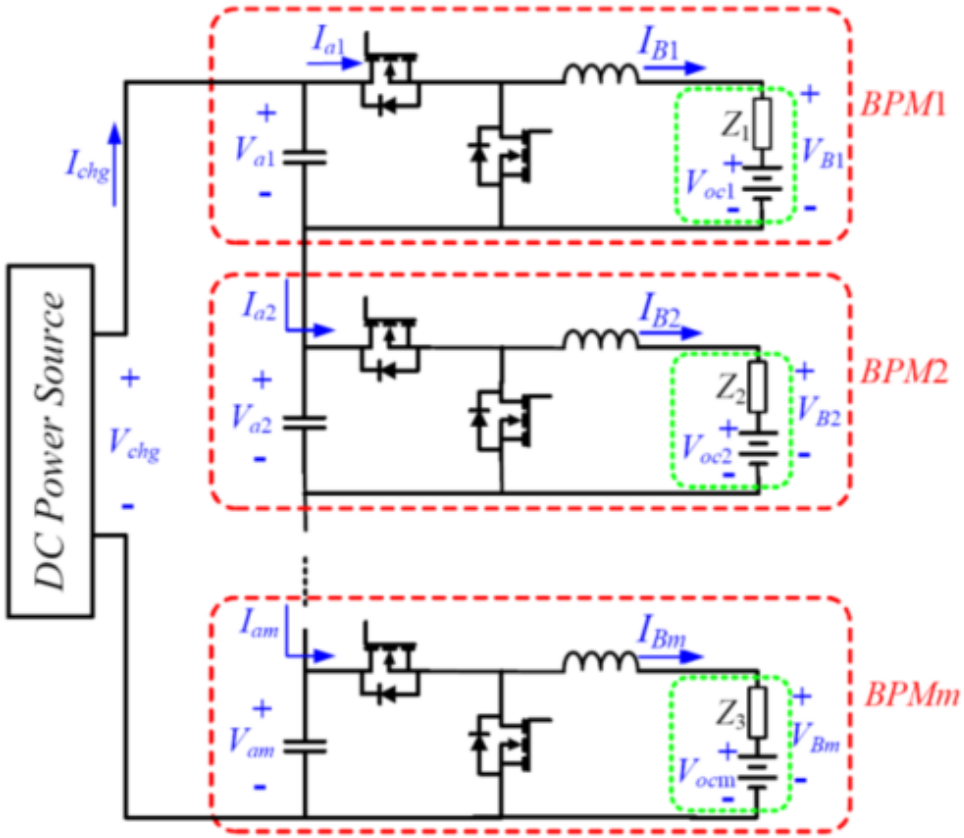

FIGURE 2.5: The buck-boost balancing system [24]

mode, the energy is transferred to the battery cells that have lower SOC from the DC power source. In the buck-boost mode, the converter removes the excess energy from the higher SOC cells and stores it in the DC link, and then retransfers it to lower SOC cells [8, 24].

2.2 Traction Drives for Battery EVs

Many types of converters are used to achieve the requirements of AC motor drive in EVs, which can be classified into three main categories:

1. **Two-level Inverters**
2. **Multilevel Inverters**
3. **Modular Multilevel Inverters**

2.2.1 Two-level Inverters

A conventional Two-level inverter is the basic inverter used by most of automobile manufacturing companies to drive their machines. The standard structure of the Two-level inverter is shown in Figure 2.6. Basically, it consists of six switches, two switches in each inverter leg. Usually, this inverter is controlled via Sinusoidal Pulse Width Modulation (SPWM) technique to generate line-line output voltage of $+V_{dc}$, $-V_{dc}$, and 0 as summarized in Table 2.1. Although, this inverter is easy to implement and control. It has many drawbacks, such as, it has high switching losses at higher switching frequencies which lead to a low efficiency, high harmonic contents in the output voltage, and may cause unbalanced DC-link capacitor voltages, and it needs external BMS to balance the series battery cells [25–27].

TABLE 2.1: Switches states of the two-level inverter

S_1	S_2	S_3	S_4	S_5	S_6	V_{ab}	V_{bc}	V_{ca}
1	1	0	0	0	1	$+V_{dc}$	0	$-V_{dc}$
1	1	1	0	0	0	0	$+V_{dc}$	$-V_{dc}$
1	0	0	0	1	1	$+V_{dc}$	$-V_{dc}$	0
1	0	1	0	1	0	0	0	0
0	1	1	1	0	0	$-V_{dc}$	$+V_{dc}$	0
0	0	1	1	1	0	$-V_{dc}$	0	$+V_{dc}$
0	0	0	1	1	1	0	$-V_{dc}$	$+V_{dc}$
0	1	0	1	0	1	0	0	0

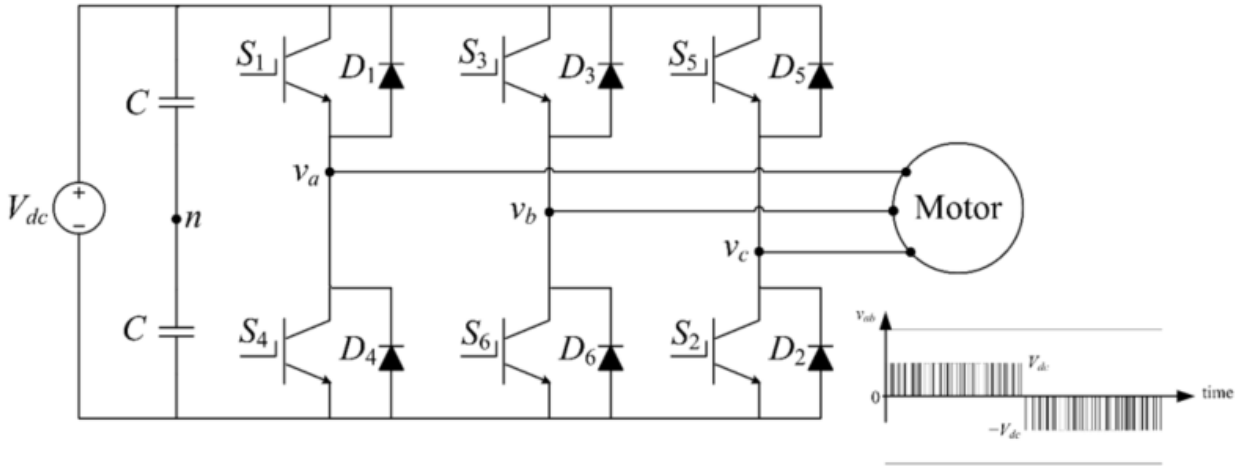

FIGURE 2.6: The two-level inverter circuit

2.2.2 Multilevel Inverters

To overcome some of the issues appeared in the Two-level inverters and to achieve the requirement for higher power and voltage drive, most of EVs companies tried to replace their Two-level inverters with multilevel inverters such as, three-level inverters, cascaded H-bridge inverters, diode-clamped inverters, flying capacitors inverters.The main idea of the multilevel inverters is to form the desired output voltage waveform by switching between several levels of DC voltages.

1. **Diode-clamped Inverters**
   Diode-clamped inverters are used as alternative to Two-level inverters. They can provide different number of output voltage levels based on the number of switches utilized in each leg. Figure 2.7 shows a Three-level NPC inverter circuit, which consists of four switches in each leg. Three-level inverters have lower switching losses at high frequency compared with Two-level inverter, low voltage rating of the switches, and reduced Total Harmonic Distortion (THD). However, three-level inverters have a main drawback of unbalanced DC-link capacitor voltages [4, 5].

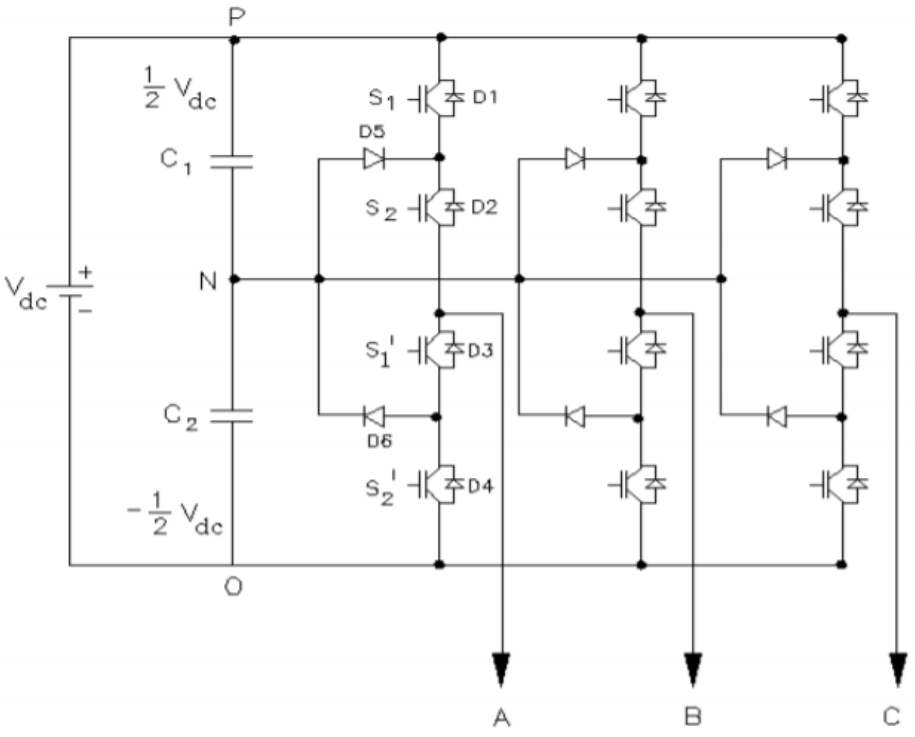

FIGURE 2.7: Three-level NPC inverter circuit

2. **Flying-capacitors Inverters**
   The configuration of this inverter is quite similar to the previous one except that, it has flying capacitors instead of diodes. N-levels flying capacitor inverter requires $2N-2$ switches and $N-1$ DC input capacitors for proper operation. Figure 2.8 shows three-level flying capacitor inverter.

   In this inverter, the maximum voltage stress across each switch is limited to one capacitor voltage which is maintained at $V_{dc}/2$. The three-level flying capacitor inverter produces three output voltage levels as follow [28]:

   (a) when switches S_{A1} and S_{A2} are turned on, it provides $V_{dc}/2$ voltage level.

   (b) when switches S_{A1}, and S_{A3} or S_{A2} and S_{A4} are turned on, the output voltage level will be 0.

   (c) when switches S_{A3} and S_{A4} are turned on, the output voltage level will be -$V_{dc}/2$.

   Main advantages of this type of inverters are:

   (a) It offers low THD at the output voltage and current.

   (b) It provides control for both active and reactive power.

   (c) It provides switch combination redundancy for balancing different voltage levels.

   However, there are some drawbacks associated with flying capacitors multilevel inverters such as:

   i. The series connected battery cells are unbalanced, so BMS must be added to the battery pack.

   ii. High level FC inverters are expensive and difficult to package with the bulky power capacitors

   iii. Excessive number of storage capacitors is required when the number of levels is high which increases the cost of the inverter.

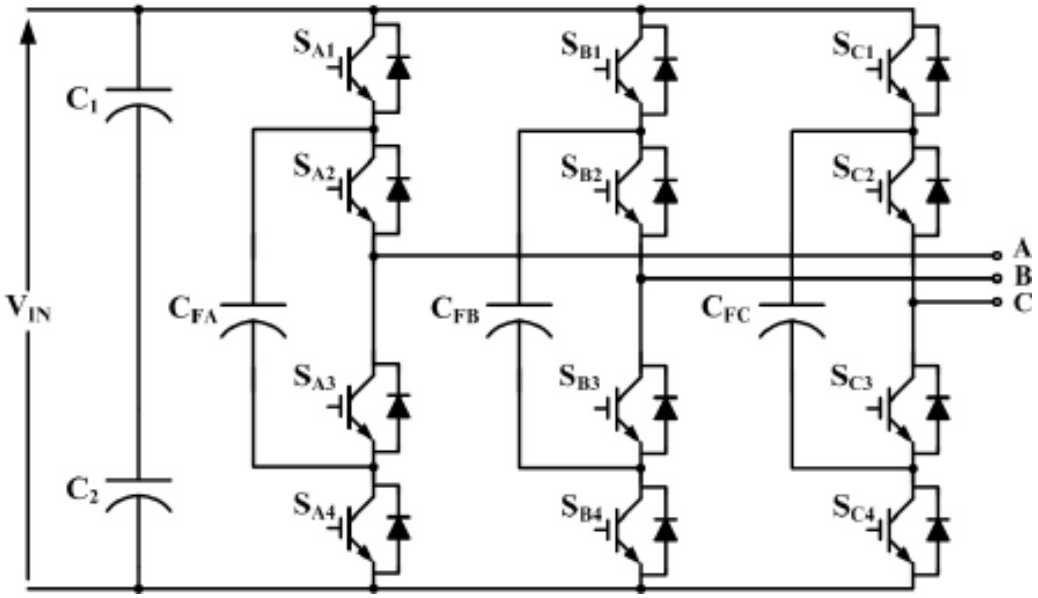

FIGURE 2.8: Three-level flying capacitor inverter

3. **Cascaded H-bridge Inverters**

   This type of inverters consists of several H-bridge inverter units connected in series in each phase of the inverter to provide a sinusoidal output voltage. The number of output voltage levels depends on the number of H-bridge units connected in each leg; if the inverter has N H-bridge units in each leg, then the output will have $2N + 1$ output voltage levels [6]. Each H-bridge unit has its own DC source which could be the battery cell for an electric vehicle system, and produces a quasi-square waveform, where each switch conducts for a half cycle.

   One of the most important applications for the cascaded H-bridge inverters is the electric vehicle motor drive systems. Figure 2.9 shows the system configuration of EV drive system implementing a cascaded H-bridge inverter. This inverter can operate in different modes: motoring, charging, and regenerative braking modes. In motoring mode, the power flows from the battery cells through the inverter to the motor. whilst, in the charging mode, the battery cells will be charged from an AC source, and the power flows through the H-bridge inverter which acts as a rectifier during this mode. In the regenerative braking mode, the cascaded H-bridge inverter acts as a rectifier recovering the kinetic energy of the vehicle and storing it in the cells.

   In general, this inverter has the same general features of other multilevel inverters including the higher number of voltage levels, reduced Total Harmonic Distortion (THD), no voltage sharing problems between devices, and reduced dv/dt. In particular, the main advantages of using the cascade inverter in an electric vehicle include:

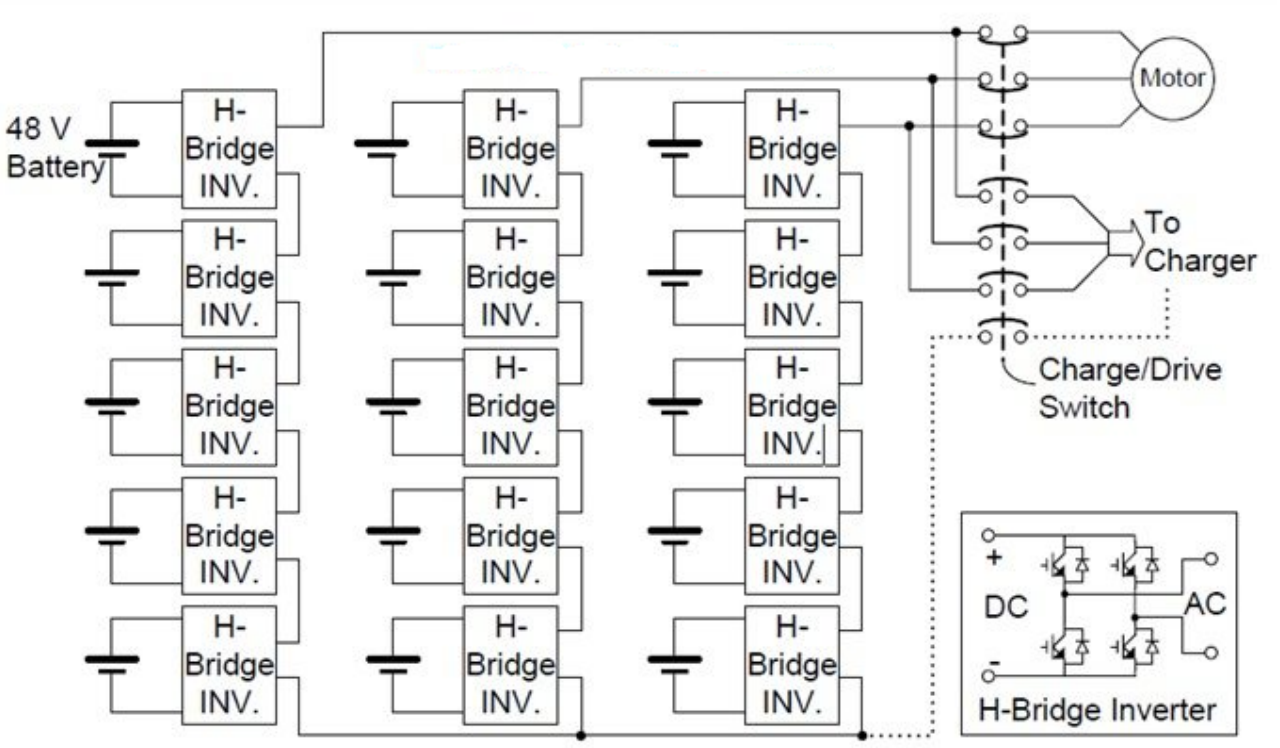

FIGURE 2.9: System configuration of an EV motor drive using cascade H-bridge inverter[6]

(a) It makes EVs more accessible and safer, since the power circuit is isolated through the switches, thus, any wiring point can be accessed safely.

(b) Traditional 230V, or 460V motors can be used.

(c) No Electro-Magnetic Interference (EMI) problem or common-mode voltage/current problem exists.

(d) Low voltage switching devices can be used.

(e) No charge unbalance problem exists in both charging and driving mode.

There are some limitations associated with using H-bridge multilevel inverters such as:

i. Each H-bridge unit needs a separate DC source, but this is not a problem for battery-powered EVs.

ii. Limited applications due to a large number of sources.

2.2.3 Modular Multilevel Inverters

Recently, Modular Multilevel Converters (MMCs) became widely used in high power applications. MMCs have many advantages over other multilevel converter topologies, such as, its modularity and scalability to meet any voltage requirement, lower losses and high efficiency, reduced THD and consequently the size of passive filter's components can be reduced, low dv/dt on devices and good voltage sharing for semiconductors. Three-phase MMC consists of three legs, each leg-phase has upper and lower arms, where the arm is composed of N identical series-connected Sub-Modules (SMs) and a series inductor L, which is necessary to limit the circulating current. The SMs within each arm are controlled to get the required AC output phase voltage [7]. Figure 2.10 shows the general structure of a MMC.

The SMs within each arm in the MMC can be built from several circuits, the most popular configuration used is the Half-Bridge (HB) circuit, which consists of two IGBTs/MOSFETs with their anti-parallel diodes, as shown in Figure 2.10(a).

Each half-bridge SM has two possible states: ON state (SM inserted) or OFF state (SM bypassed). When $S1$ is turned on, the SM will be in the ON state, and the output voltage will equal to the capacitor voltage. If $S2$ is turned on, the SM will be in the OFF state, and the output voltage will equal zero. HB circuit can work also in two quadrants as it can handle reverse current [7, 29, 30].

The SM in the MMC can be also constructed using full-bridge circuit, which consists of four IGBTs/MOSFETs as shown in Figure 2.10(b). The output voltage of the full-bridge SM is either equal to the capacitor voltage or zero voltage, depending on the switching states of the four switches. This topology has higher losses and cost compared with HB topology as the number of switches is doubled.

Other SMs circuits can be used to construct the arms of the MMC such as, clamp-double circuit, three level inverter which is composed from either three-level Neutral-Point-Clamped (NPC) or three-level Flying Capacitor (FC), and five-level cross-connected circuit. The comparison between these configurations in terms of losses, DC-fault current handling is given in Table 2.2.

TABLE 2.2: Comparison between different SMs circuits [7]

SM circuit	DC-fault current handling	losses
Half-bridge	No	Low
Full-bridge	Yes	High
Clamp-double	Yes	Moderate
Three-level FC	No	Low
Three-level NPC	No	Moderate
Five-level cross connected	Yes	Moderate

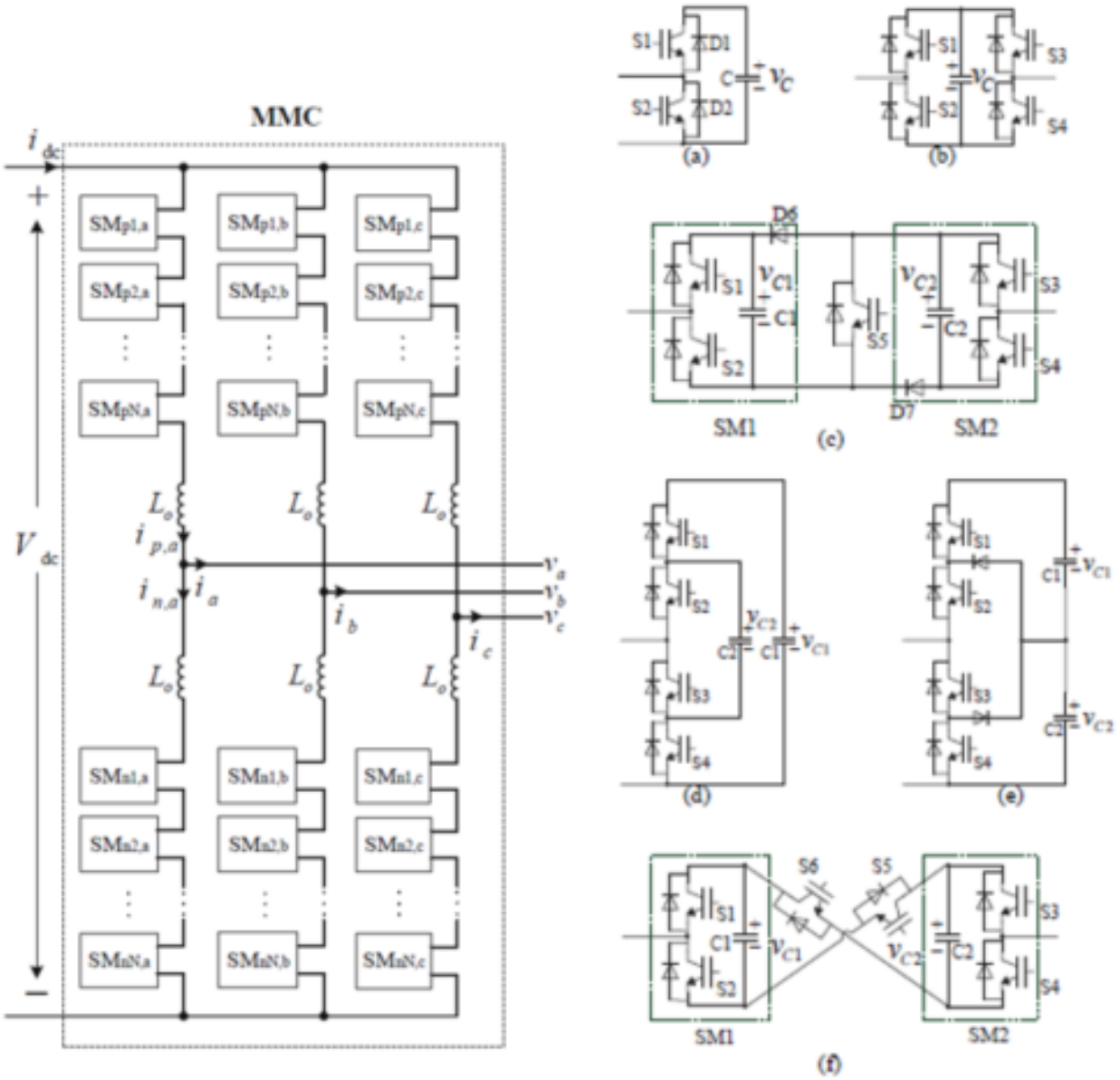

FIGURE 2.10: The basic structures of MMC (a) Half-Bridge, (b) Full-Bridge, (c) Clamp-Double, (d) Three-level FC, (e) Three-level NPC, and (f) Five-level cross-connected SM [29]

The Double-Star Modular Multilevel Converters (DS-MMCs) are recently used in battery electric vehicles (BEVs). In this configuration, there is no common DC-link, and the battery cells are integrated with the SMs of the converter (bidirectional DC-DC buck converter). Figure 2.11 shows the structure of the DS-MMC with half-bridge chopper cells [9, 10]. This topology has many advantages such as, it offers low THDs of output voltages and currents, it is flexible on the energy management, it has four quadrants of operation, it operates with reduced switching losses since it can operate at a low switching frequency. However, it has some disadvantages, as it needs a special controller to monitor and balance capacitor

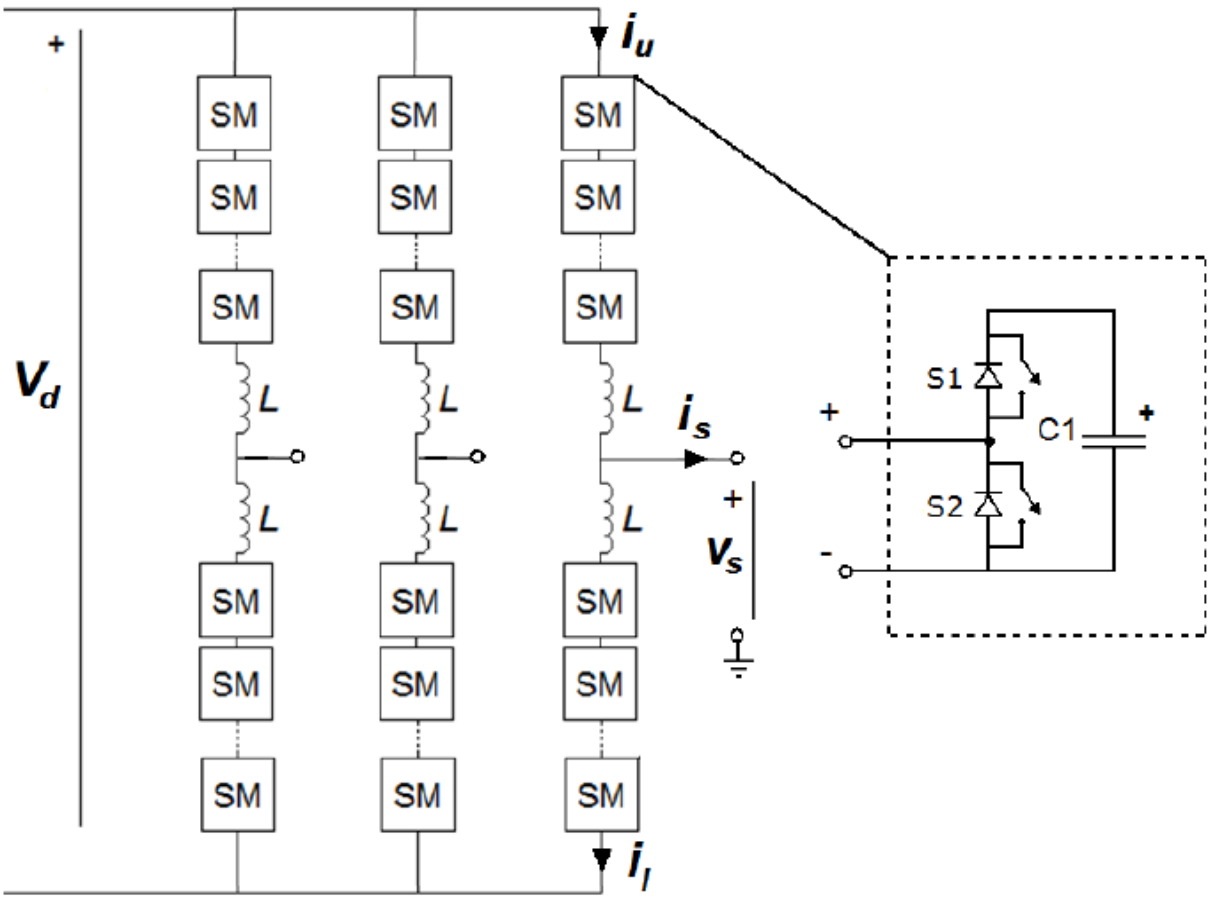

FIGURE 2.11: The DS-MMC with half-bridge chopper cell

voltages, the circulating current contains double fundamental frequency component, which can stress the switches of the converter [10], it has high conduction losses, the number of SMs and hence the number of semiconductor devices required will be very large since one SM is used for each battery cell. Moreover, it has high-frequency pulsed current in each battery cell which reduces their life-time. Table 2.3 summarizes the advantages and disadvantages of the aforementioned toplogies:

TABLE 2.3: Advantages and disadvantages of several EV drive topologies [6, 25, 26, 28]

Topology	Advantages	disadvantages
NPC	• Low THD of output voltages and currents.	• The clamping diodes have unequal reverse voltage blocking ratings, so excessive clamping diodes are required.
	• It does not require a high switching frequency to supply nearly sinusoidal currents, which means lower switching losses and higher efficiency.	• The complexity of the NPC inverters increases when the number of output voltage levels increases.
	• The voltage supported by each semiconductor switch is significantly small.	• The switching devices have unequal ratings.
	• The converter control method is simple.	• The capacitor voltages between the different inverter levels are unbalance. • The series connected battery cells are unbalanced, so BMS must be added to the battery pack.
FC	• It offers low THD of output voltages and currents.	• Excessive number of storage capacitors is required when the number of levels is high.
	• It can provide continuous operations even with the failure of one level of the structure because of the large amount of storage capacitors.	• High level FC inverters are expensive and difficult to package with the bulky power capacitors.
	• It provides switch combination redundancy for balancing different voltage levels.	• The inverter control can be very complicated and the switching losses are high.

Continued on next page

Table 2.3 – *Continued from previous page*

Topology	Advantages	Disadvantages
	• The voltage supported by each semiconductor switch is significantly smaller than conventional two-level inverter. • Both real and reactive power flow can be controlled.	• The series connected battery cells are unbalanced, so BMS must be added to the battery pack.
CHB	• The harmonic contents decreases as the number of levels increases and filtering requirements are reduced. • It requires less number of components to obtain the same number of output voltage levels. • Optimized circuit layout and packaging are possible because each level has the same structure. The series of H-bridges made for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply. • The switching devices have equal ratings.	• It needs separate dc sources, but this is not a problem for battery EVs. • When batteries, instead of cells, are used as dc sources, variations between cells and exposure to different charge and discharge rates lead to unequal SOCs of cells within the batteries. Over extended cycling, this can cause premature failure of the pack due to the over- or undercharging of individual cells. • In Y-connected CHB, it is difficult to balance the inverter legs using circulating currents because this will result in distorted motor currents. This disadvantage is partially mitigated by D-connected CHB where zero-sequence current can be used. However, it is not possible to balance independently the converter legs because the same zero sequence current will flow through the three legs.

Continued on next page

Table 2.3 – *Continued from previous page*

Topology	**Advantages**	**Disadvantages**
	• Soft switching techniques can be used to reduce switching losses and device stresses. • It can be used to drive the traction motor from the battery, allowing continuous operations even with the failure of one level of the structure.	
DS-MMC	• It offers low THDs of output voltages and currents. • Easy to be expanded with modular structure design. • Flexible on the energy management. • Fault-tolerance capabilities. • Four-quadrant operations. • It has low switching frequencies of the individual switches, which results in reduced switching losses. • It allows the recharge of the battery units either from dc or single phase ac power sources.	• It has high conduction losses. • Since one sub-module is used for each battery cell, the number of Sub-Modules and hence the semiconductor devices required will be very large. • High-frequency pulsed current in each battery cell and this reduces their life-time. • It needs special controllers to balance the converter legs and arms.

A significant improvement to the present topologies could be done using a Single Star-Modular Multilevel Converter (SS-MMC), which is proposed in this thesis to overcome some of the issues associated with the earlier MMCs. The proposed converter basically eliminates the lower arms of the conventional MMC with the inductors. Consequently, the system's size, cost and losses will be reduced. In addition, the SMs of this converter will have a special designed DC-DC converter, which can boost the cells voltage and allowing drawing of current in both directions and enabling the operation of the machine in both modes (motoring and regenerating). The usage of the bidirectional DC-DC boost converter SM integrated with the bidirectional DC-DC buck converter may decrease the number of required

cells, and allow operation with a lower switching frequency, which consequently reduces the switching losses of the converter.

Chapter 3

Single Star-Modular Multilevel Converter (SS-MMC)

Based on the preceding review illustrated throughout the accomplished works in BMSs topologies and the traction drives introduced in the previous chapter with their limitations, this chapter proposes a new conversion system, Single Star Modular Multilevel Converter (SS-MMC), on a level discussed in terms of its structure and principle of operation. Also, it will present the Li-Ion cell's dynamic model, which is usually used as energy source in the EV. In addition, the modulation technique used in driving the converter will be discussed. Moreover, current controller design and implementation will be discussed.

3.1 Converter Structure

The system structure with the proposed conversion system is shown in Figure 3.1. The system consists mainly of the multilevel conversion system used to drive the EV's motor with the required special controllers. The system operates in two modes: charging mode and discharging mode. In the charging mode a charge switch is used to connect the SS-MMC to the grid to charge the battery cells at unity power factor using a standard decoupled active and reactive power control which is combined with the voltage-balance controllers to maintain the balance condition at the battery cells during charging. To optimize energy transfer, a Phase Locked Loop (PLL) system will be used to estimate the grid frequency and phase angle. In the discharging mode, the SS-MMC will drive the EV's motor with balancing the battery cells based on their voltage levels. The converter consists of three legs where each leg consists of n series connected Sub-Modules (SMs). Each SM connected directly at the terminals of the battery cell and is composed of a bidirectional boost converter followed by DC-DC buck converter.

The bidirectional boost converter is meant to establish a governed stage for power flow and charge-discharge control, the use of the converter as a door way for cell charging and

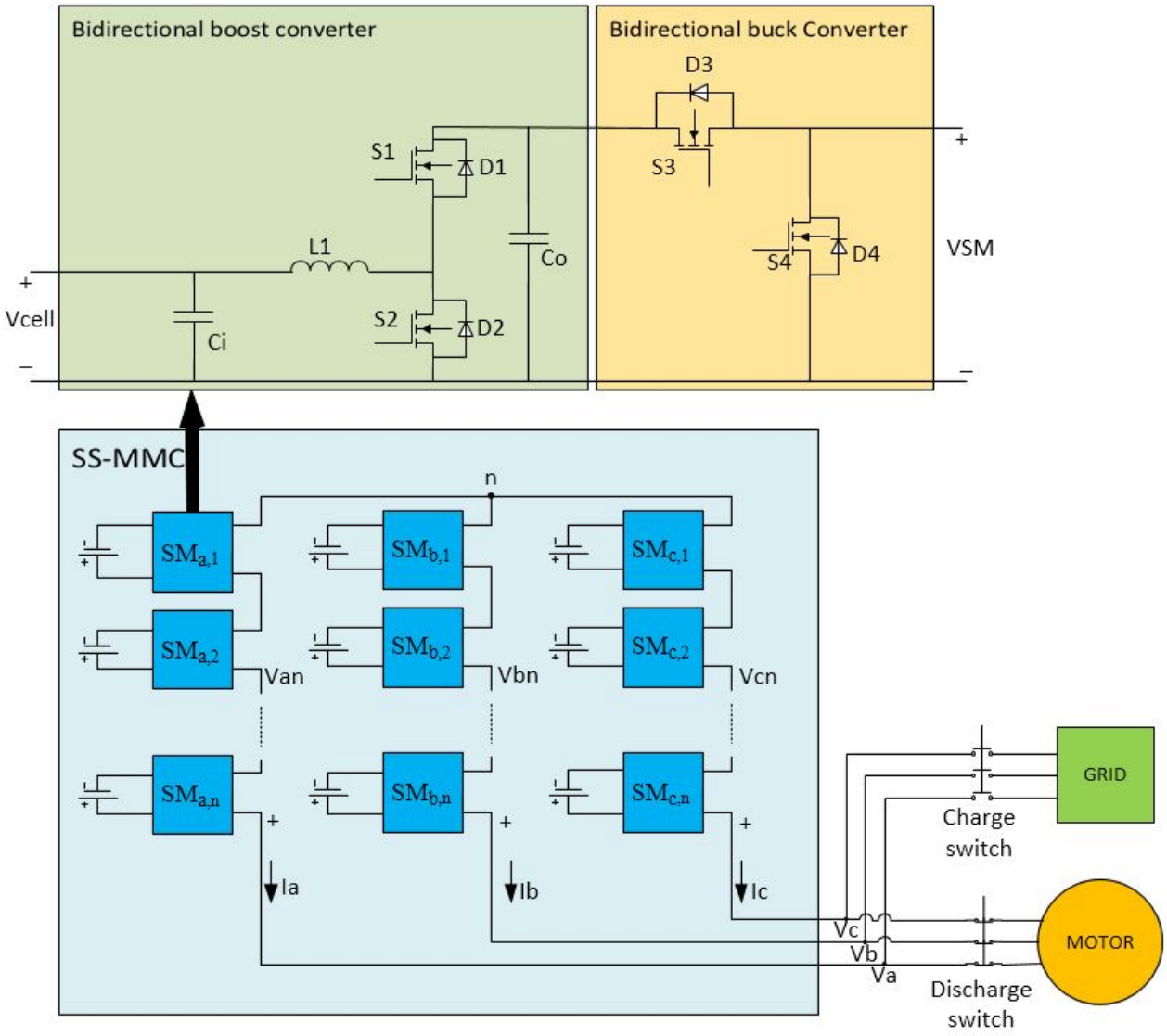

FIGURE 3.1: The block diagram of the proposed SS-MMC topology

drawing power at demand provides a dynamic range for the set of combinations capable of providing a certain output voltage level. Moreover, an added advantage of maintaining continuous current with reduced surges at the cells terminals would be applicable due to the presence of the inductive energy storage element found in the converter topology.

3.1.1 Bidirectional DC-DC Boost Converter

Figure 3.2 shows the proposed Bidirectional DC-DC boost converter connected with a battery cell. This topology operates in two modes (boost and buck modes). For the motor drive operations the converter step-up stage is used to step up the battery voltage and control the inverter input. The boost operation is achieved by operating S_2 with the anti-parallel diode

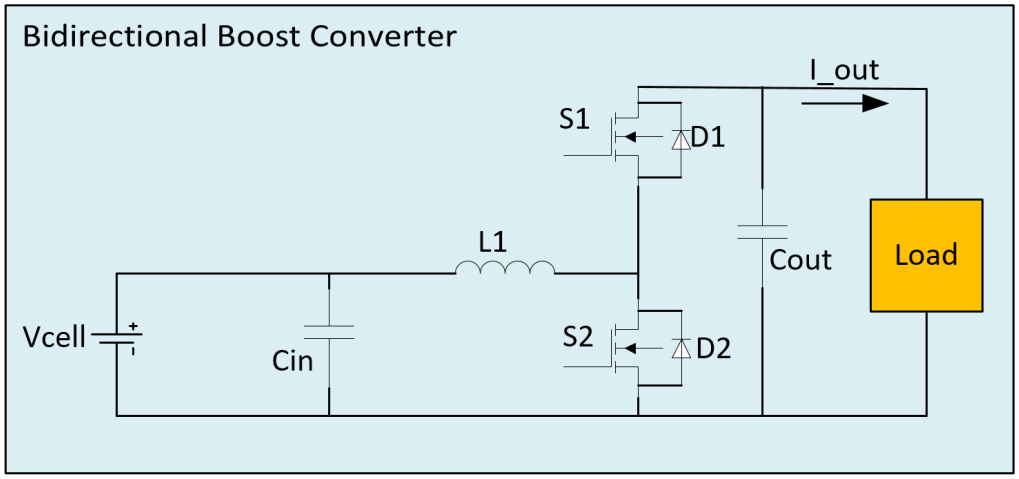

FIGURE 3.2: Bidirectional boost converter topology

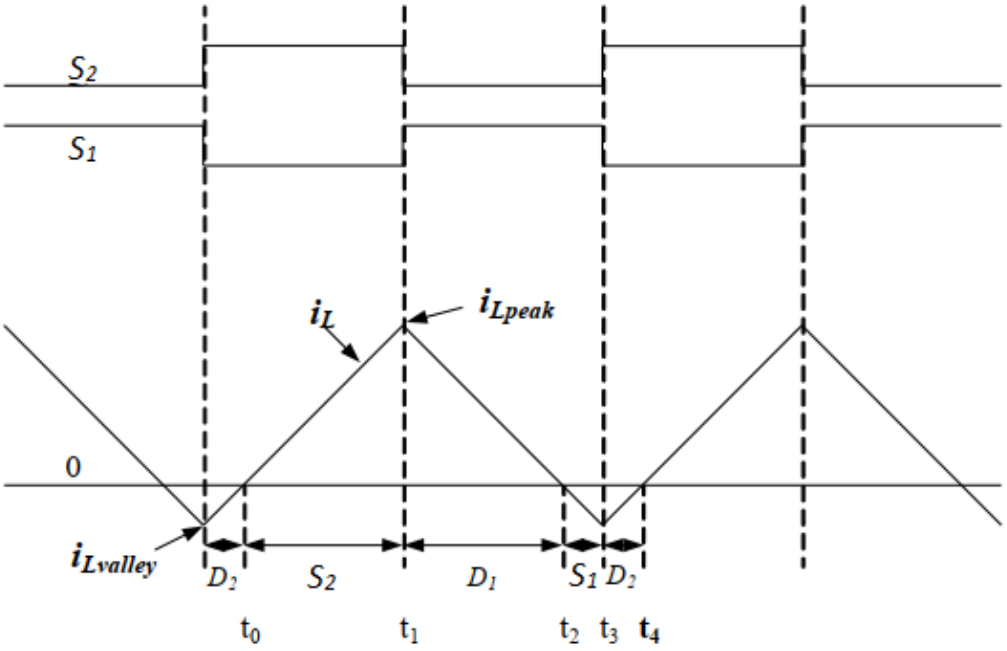

FIGURE 3.3: Switches gate signals

D_1 serving as the boost-mode diode. When the direction of power flow is reversed, the system functions as a buck converter with both S_1 and the anti-parallel diode D_2 acting as the buck-mode diode. It is noted that, the two modes operate at opposite inductor current directions. The converter works in the first quadrant when S_2 is OFF, diode D_2 is not conducting and S_1 is ON. If the switch S_1 is OFF, S_2 is ON and diode D_1 is not forward biased, then the converter operates in the second quadrant. The gate signals of the the switches are shown in Figure 3.3 [31–35]. There are four possible steady state modes of operation for different intervals for this converter. These four possibilities are:

- Interval 1 (t_0-t_1): When the instantaneous current i_o = 0, the switch S_2 conducts and

continues to do so till t_1, as shown in Figure 3.4(a). D_1 and D_2 are reversed biased during this time interval and the converter operates in boost mode while the inductor current increases.

- Interval 2 (t_1-t_2): Both switches in this interval are turned OFF, and the body diode D_1 of the upper switch S_1 starts conduction, as shown in Figure 3.4(b). The instantaneous inductor current i_o decreases with time till t_2, while the output voltage of the converter increases as the converter operates in boost mode during this time interval.

- Interval 3 (t_2-t_3): At t_2 the i_o becomes zero, and S_1 starts conduction with D_1 and D_2 reversed biased, as shown in Figure 3.4(c). During this time interval the converter operates in buck mode.

- Interval 4 (t_3-t_4): In this time interval both converter switches S_1 and S_2 are turned OFF and the diode D_2 of the lower switch starts conducting, as shown in Figure 3.4(d).

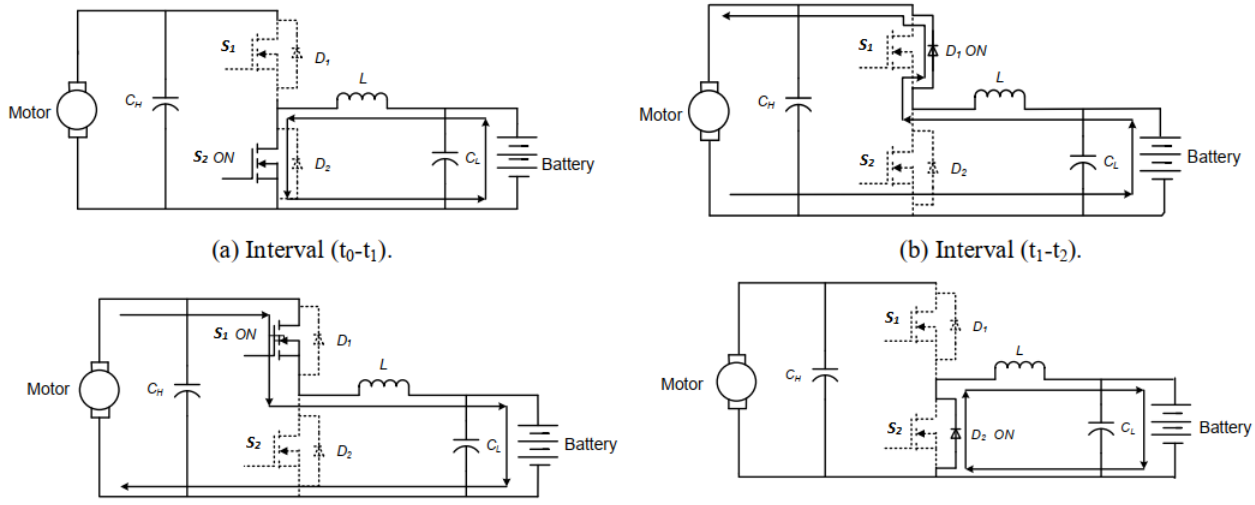

FIGURE 3.4: Converter operating modes

During the operation in the first interval (boost mode), the voltage across the inductor will be:

$$V_L = L\frac{di}{dt} \tag{3.1}$$

while the inductor ripple current given by:

$$\Delta I = \frac{V_{cell}DT}{L} \tag{3.2}$$

where,
D: duty cycle

T: switching period
Deriving the instantaneous output voltage yields:

$$V_{boost} = \frac{V_{cell}}{1 - D} \tag{3.3}$$

where,
V_{cell} is the input battery voltage
V_{boost} is the boost's output voltage.

According to equation 3.3, the operation with high duty ratios lead the converter to an unstable region, as the efficiency of the boost converter is inversely proportional to the duty cycle. Thence, D must not exceed 0.8 value to ensure the operation under stability.

3.1.2 Bidirectional DC-DC Buck Converter

A bidirectional DC-DC buck converter is connected in each SM across the output terminals of the bidirectional boost converter as was shown in Figure 3.1. The main function of using such a converter is to achieve the switching modes of the SMs based on the operating switch (S_3 and S_4), when S_3 is turned ON for a certain SM, the SM is considered to be ON meaning that it provides an output voltage at its terminals relative to the voltage level provided from the previous bidirectional boost. For the second mode, when S_4 is turned ON the SM is considered to be OFF and the output voltage of the converter is zero due to a bypass short exerted by S_4. The possible switching states of basic structure of the converter is shown in Table. 3.1. This converter provides the ability to reverse the power flow allowing the input battery cell to be charged and discharged during specific intervals [25].

TABLE 3.1: Switching states of the DC-DC buck converter.

S_3	S_4	V_{SM}	Current Direction	Power Path	Cell state
1	0	V_{boost}	$i_{SM} > 0$	S_3	discharging
1	0	V_{boost}	$i_{SM} < 0$	D_3	charging
0	1	0	$i_{SM} > 0$	D_4	unchanged
0	1	0	$i_{SM} < 0$	S_4	unchanged

3.1.3 Operating Principle

The number of SMs in each leg of the SS-MMC converter determines the number of levels at the output voltage. Assuming that, converter has n SMs in each leg, the maximum voltage across the leg will be nV_{boost} as the voltage changes between zero and nV_{boost}, where V_{boost} is the boosted output voltage given by the bidirectional boost converter, which means that it

has a DC component across the leg as illustrated in Figure 3.5. Therefore, the neutral point of the converter and the load must be separated to cancel the DC component. The line-to-line output voltage of the converter will have $n + 1$ levels. One of the advantages of using such a topology is the ability to reduce the harmonic content appearing in the output waveforms by increasing the number of SMs. Moreover, having the bidirectional boost serving as the input stage of the buck allows a certain flexibility in considering how exactly to achieve a compromise between the number of SMs and maintaining the required voltage level in each phase with the consideration of a minimum distortion due to harmonic content for a given number of SMs. The THD gives an indication about the harmonic content in the output voltage waveform, which is defined as:

$$THD = \sqrt{\frac{(V^2) - (V_1)^2}{(V_1)^2}} \tag{3.4}$$

Where, V_1 is the rms value of the fundamental frequency of the output voltage, and V is the rms value of the whole waveform of the output voltage.

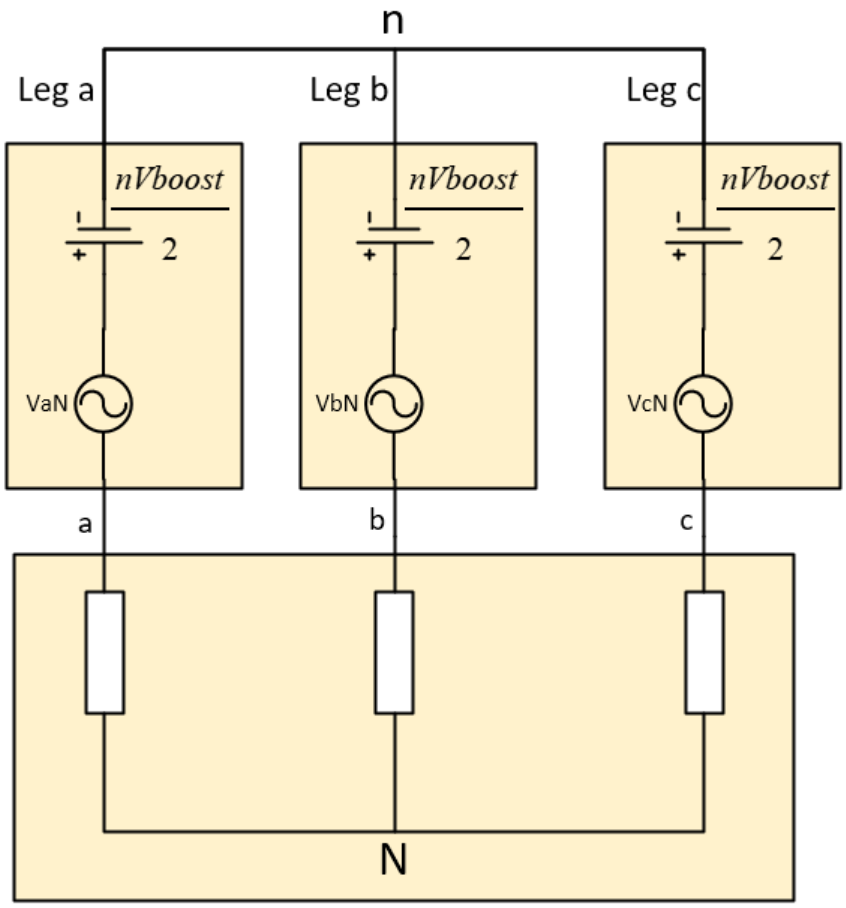

FIGURE 3.5: The equivalent circuit of the proposed converter

The direction of current flow through the cell determines the state of the cell (charging or discharging). The load current flowing through the converter's leg is the same current flowing through the turned ON SMs. The line-to-line output voltage can be expressed as:

$$\begin{aligned} v_{ab} &= v_{aN} + \frac{nV_{boost}}{2} - \frac{nV_{boost}}{2} - v_{bN} = v_{aN} - v_{bN} \\ v_{bc} &= v_{bN} + \frac{nV_{boost}}{2} - \frac{nV_{boost}}{2} - v_{cN} = v_{bN} - v_{cN} \\ v_{ca} &= v_{cN} + \frac{nV_{boost}}{2} - \frac{nV_{boost}}{2} - v_{bN} = v_{cN} - v_{aN} \end{aligned} \tag{3.5}$$

where V_{kN} is the converter phase k voltage with respect to the motor neutral point, N. The leg voltage V_{kn} of phase k with respect to the converter neutral point can be expressed as shown in equation (3.6):

$$v_{kn} = v_{kN} + \frac{nV_{boost}}{2}; \qquad -\frac{nV_{boost}}{2} \leq v_{kN} \leq \frac{nV_{boost}}{2}, \qquad k \in a, b, c \tag{3.6}$$

3.1.4 Converter Modulation Strategy

The proposed converter uses a Carrier Disposition-third harmonic injection Pulse Width Modulation (CD-THIPWM) technique to ensure a reduced harmonic distortion imposed by the flatness of the switching voltage levels.

The principle of operation for this technique is using n SMs for each phase to provide an $n + 1$ line-to-line levels as an AC output for the converter. The modulation is achieved by comparing a required reference sinusoidal input of a certain amplitude and frequency with multiple carrier signals each is assigned to a certain SM in order to determine the number of active SMs in each leg at a certain instant.

Some definitions related to this scheme are summarized by the following:

- The frequency modulation ratio: is defined as the ratio of the carrier frequency to the modulating signal frequency, and it is given by:

$$M_f = \frac{f_{carrier}}{f_{modulating}} \tag{3.7}$$

- Amplitude modulation index: is the ratio of the amplitude of modulating signal to the amplitude of the carrier signal, and it is given by:

$$M_a = \frac{V_{m,modulating}}{V_{m,carrier}} \tag{3.8}$$

In this modulation topology, a third harmonic component is injected into the modulating sinusoidal signal to increase the maximum peak value of the converter phase voltage without causing over-modulation. Therefore, the modulating wave signals v_a^*, v_b^*, and v_c^* are given by eq. (3.9):

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = M \begin{bmatrix} sin(\theta) + h_3 sin(3\theta) \\ sin(\theta - 2\pi/3) + h_3 sin(3\theta) \\ sin(\theta + 2\pi/3) + h_3 sin(3\theta) \end{bmatrix}; \qquad \theta = \omega t + \theta_v \tag{3.9}$$

where ω is the electric radian frequency of the modulating wave signals, θ_v is the phase angle of the modulating wave, h_3 is the percentage value of the injected third harmonic component, and M represents the modulation index of the converter and it is defined by eq. (3.10):

$$M = \frac{2V_m}{nV_{boost}}; \qquad 0 \leq M \leq 1 \tag{3.10}$$

where V_m represents the peak value of the output phase voltage. The maximum peak value of the converter output phase voltage is obtained when M = 1:

$$V_{m,max} = \frac{nV_{boost}}{2} \tag{3.11}$$

where V_{boost} is the output voltage of the boost converter.

To avoid over-modulation, the peak value of the modulating wave must be less than 1:

$$F(h, \theta) = max[M_{max} sin(\theta) + h_3 M_{max} sin(3\theta)] = 1 \tag{3.12}$$

To find the extreme point of modulating wave, partial derivatives must be taken with respect to h_3 and θ as follow:

$$\begin{aligned}
&\frac{\partial (V_a)^*}{\partial h_3} = 0 \Rightarrow \frac{\partial}{\partial h_3}[Msin(\theta) + h_3 Msin(3\theta)] = 0 \\
&Msin(3\theta) = 0 \Rightarrow sin(3\theta) = 0 \Rightarrow 3\theta = \pi \Rightarrow \theta = \frac{\pi}{3} \\
&\frac{\partial (V_a)^*}{\partial \theta} = 0 \Rightarrow \frac{\partial}{\partial \theta}[Msin(\theta) + h_3 Msin(3\theta)] = 0 \\
&Mcos(\theta) + 3h_3 Mcos(3\theta) = 0 \\
&cos(\theta) + 3h_3 cos(3\theta) = 0 \\
&cos(\frac{\pi}{3}) + 3h_3 cos(\pi) = 0 \\
&\frac{1}{2} - 3h_3 = 0 \Rightarrow h_3 = \frac{1}{6}
\end{aligned} \tag{3.13}$$

By substituting the results of eq.(3.12) in eq.(3.13), the maximum modulation index will be:

$$\begin{aligned} &F(h,\theta) = max[M_{max}sin(\theta) + h_3 M_{max}sin(3\theta)] = 1 \\ &M_{max}sin(\frac{\pi}{3}) + h_3 M_{max}sin(3\frac{\pi}{3}) = 1 \\ &M_{max}sin(\frac{\pi}{3}) + h_3 M_{max}sin(\pi) = 1 \\ &M_{max}sin(\frac{\pi}{3}) = 1 \\ &M_{max} = \frac{2}{\sqrt{3}} = 1.155 \end{aligned} \tag{3.14}$$

as a results, with the use of CD-THIPWM modulation technique it is shown that the maximum value of the fundamental component of the reference signal can reach an additional 15.5%, and the injected third harmonic component is 1/6 of the maximum value of the fundamental. Therefore, this modulation scheme is able to generate the required output voltage which can be generated by the traditional CD-SPWM technique with a reduced number of SMs by a factor of 13.5%, and this will help in increasing the efficiency of the converter and reduces the cost of implementation. Figure 3.6 shows the CD-THIPWM scheme, the modulating signals compared with the carrier signals to determine the number of active SMs in each leg. Carriers shifted by 2/n in the range between -1 and 1, and each carrier has $2/n$ peak-peak value and switching frequency f_{sw}. The point of intersection between the modulating wave with the carrier signal are defined as the points where the level is created, by generating proper control signals for the converter switches. The maximum line-line voltage can be generated with the use of this scheme is given by:

$$V_{L-L} = \frac{1}{\sqrt{2}} \frac{n}{1-D} V_{boost} \tag{3.15}$$

With choosing the duty cycle to have its maximum value of 0.8, the minimum number of SMs of each leg can be determined by:

$$n_{min} = 0.283 \frac{V_{L-L,max}}{V_{cell}} \tag{3.16}$$

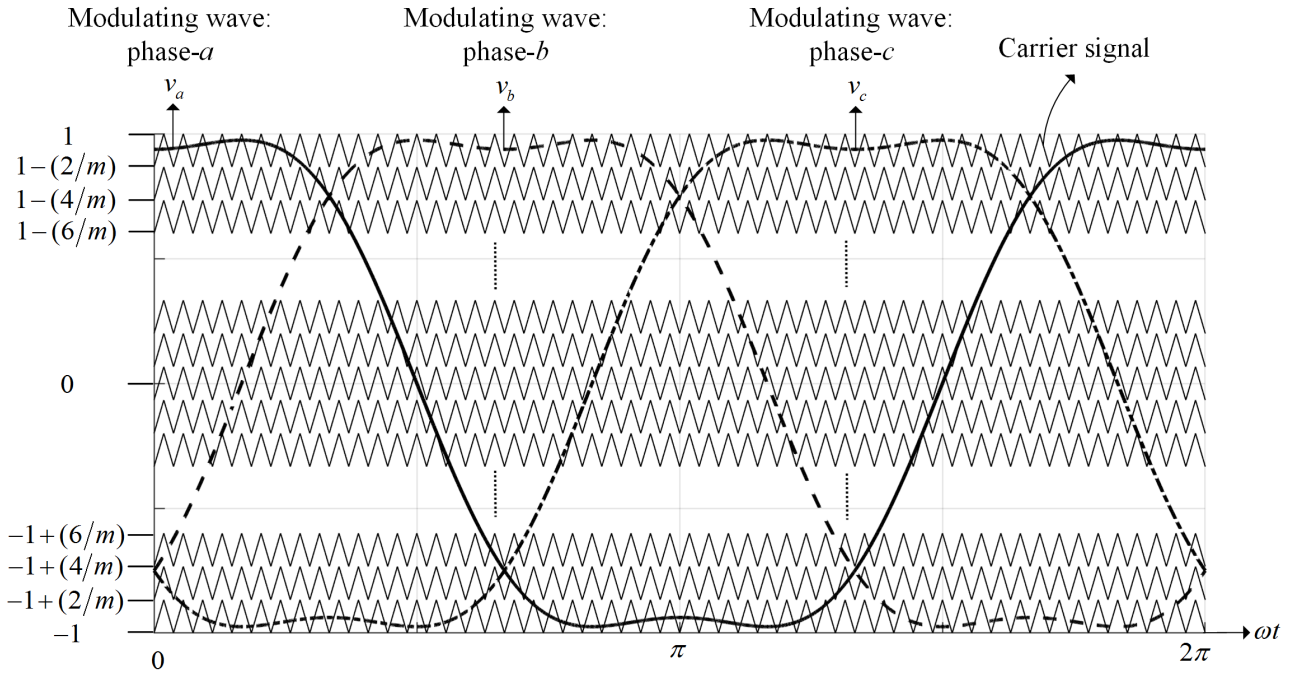

FIGURE 3.6: The CD-THIPWM scheme

3.1.5 Capacitor Voltage Balancing Algorithm

Unbalanced voltage distribution causes unequal stresses among switches and capacitors, which may lead to the failure of switches, the damage of some capacitors and the over-charging of others [36]. Modular multilevel converters have a challenging predicament manifested in maintaining a balanced voltage distribution among the capacitors of the SMs. However, the presented converter provides the particularity of freedom to turn on and off any SM. Hence, a balancing algorithm was used to ensure preserving the capacitors' voltages at their nominal values by finding the best switching combinations during each switching cycle.

The function of the capacitors' voltages balancing controller is to balance all capacitors' voltages in each converter leg. The capacitors' voltages were measured and then sorted in a descending order via a processor according to their voltage levels. During the positive half cycle of the motor current, the capacitor current is positive and the capacitor operates in the discharging mode. In this case, the SMs with the highest voltages are switched on. In the next half cycle of motor current, the capacitors current becomes negative and the capacitors operates in the charging mode. In this case, the SMs with the lowest capacitors' voltages are selected to be switched on. Using this method, the balancing of capacitors' voltages is guaranteed within the leg and all capacitors will have the same voltage. Figure 3.7 shows the flow chart for the algorithm used for balancing capacitors voltages within the SMs of the converter.

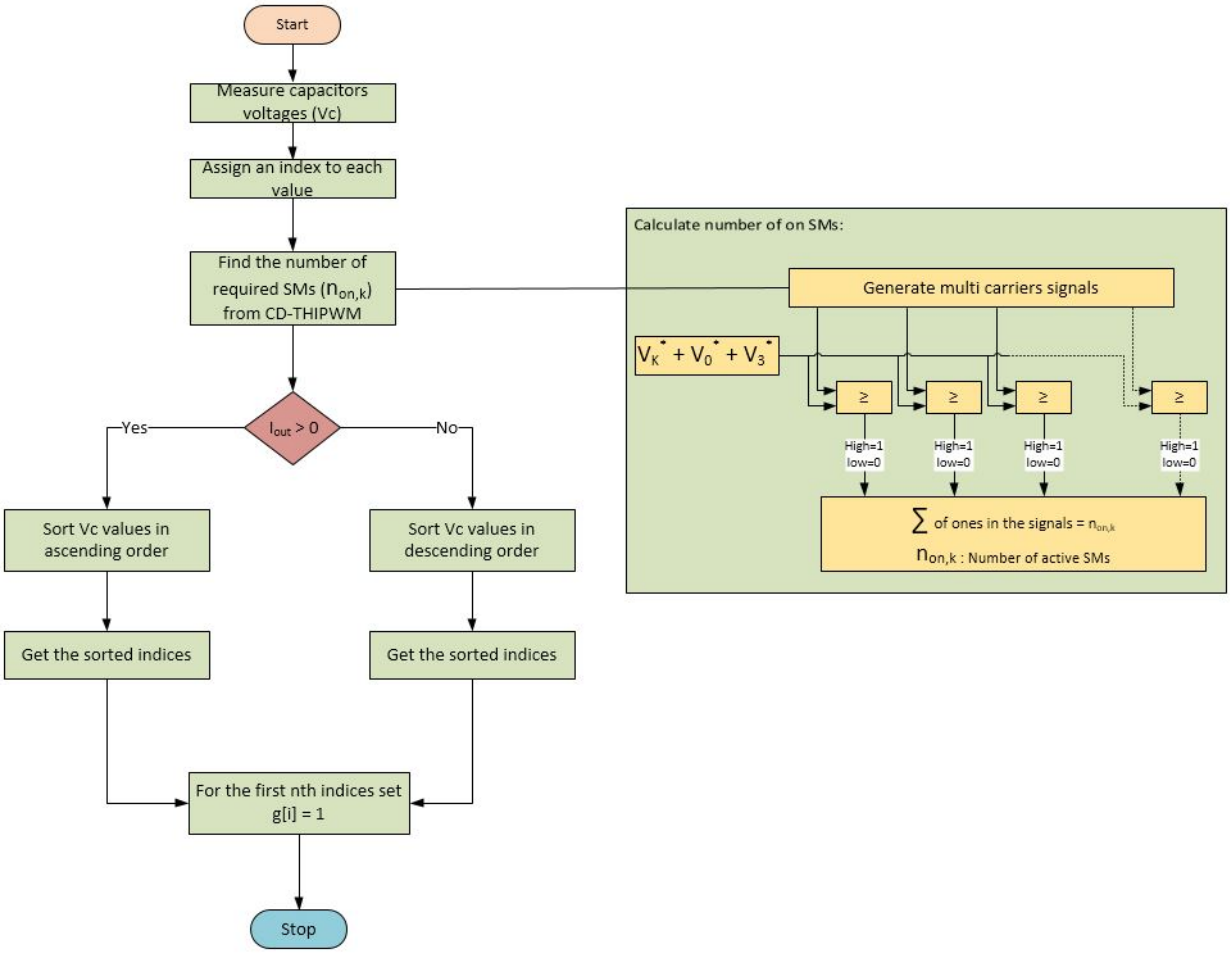

FIGURE 3.7: Capacitor voltage balancing algorithm flow chart

3.1.6 The lithium-ion Electrical Battery Model

In the BEVs, the Li-ion battery cells are usually used because they have high energy density compared with Nickel-cadmium, Nickel metal and lead acid battery cells [17]. This section will introduce the dynamic model of Li-ion battery cells. The state of charge of the cells gives an indication about its available capacity. It is defined as the ratio of the available capacity of the battery to its maximum available capacity [37]:

$$SOC = \frac{Q - q}{Q} \tag{3.17}$$

where, q is the charge absorbed from the cell in [Ah], and Q is the capacity of the cell in [Ah]. The SOC is simply estimated using current integration method [37]:

$$SOC = SOC_i - \frac{1}{3600Q} \int idt \tag{3.18}$$

where, SOC_i is the initial SOC of the cell in [%], and i is the current drawn from the cell in [A]. The Li-ion cells can be modelled during discharge and recharge modes using battery dynamic model for EV applications which is given in [38] as:

$$\begin{aligned} V_{cell} &= V_o - R_i i_{cell} - K\frac{Q}{Q-q} i_{cell} - K\frac{Q}{Q-q} q + Ae^{-Bq}; \quad i_{cell} > 0, \quad \text{discharge mode} \\ V_{cell} &= V_o - R_i i_{cell} - K\frac{Q}{\frac{Q}{10}+q} i_{cell} - K\frac{Q}{Q-q} q + Ae^{-Bq}; \quad i_{cell} < 0, \quad \text{recharge mode} \end{aligned} \tag{3.19}$$

where, V_{cell} is the actual cell voltage in [V], V_o is the cell open circuit voltage in [V], R_i is the internal resistance of the cell in $[\Omega]$, i_{cell} in the supplied current by the cell in [A], A and B are empirical constants, k is the polarization constant in [V/Ah], Q is the cell capacity in [Ah], and q is the absorbed charge from the cell in [Ah]. In this model. the temperature and self-discharging effects are ignored, the internal resistance and the capacity of the cell are assumed to be constant and independent of the cell current.

3.1.7 Current control in SS-MMC

This section intends to discuss the design and implementation of a current controller on the proposed SS-MMC topology. The addition of the current controller provides full closed loop control on the output current and power. The design will be implemented in the rotating reference frame dq-axis, Park transformation is needed to transform the output currents from abc to dq frame. Assuming the load is static and consists of Resistor and inductor, the current controller was designed as follow:

The phase voltages, V_{abc}, are given by:

$$V_{abc} = Ri_{abc} + L\frac{di_{abc}}{dt} \tag{3.20}$$

Where,
i_{abc} = $[i_a \quad i_b \quad i_c]^T$ is the phase currents vector.
R is the resistance of the static load.
L is the inductance of the static load.

By multiplying equation 3.20 by the Clarke transformation matrix, the stationary reference frame voltage components were given:

$$V_{\alpha\beta} = Ri_{\alpha\beta} + \frac{di_{\alpha\beta}}{dt} \tag{3.21}$$

In order to get the dq-axis decoupled voltage components, Park transformation matrix is used as given in equation 3.22:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} X \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{3.22}$$

Thus, direct and quadrature voltage components were derived and expressed in equation 3.23:

$$\begin{aligned} V_d &= Ri_d + \omega L i_q + L\frac{di_d}{dt} \\ V_q &= Ri_q - \omega L i_d + L\frac{di_q}{dt} \end{aligned} \tag{3.23}$$

Then, equation 3.23 can be re-written as:

$$\begin{aligned} V_d &= U_d^* + \omega L i_q, \quad where, \quad U_d^* = Ri_d + L\frac{di_d}{dt} \\ V_q &= U_q^* - \omega L i_d, \quad where, \quad U_q^* = Ri_q + L\frac{di_q}{dt} \end{aligned} \tag{3.24}$$

The terms U_d^* and U_q^* were used to design the dq-axis current controllers as it is described below:

$$U_{dq}^* = Ri_{dq} + L\frac{di_{dq}}{dt} \tag{3.25}$$

In order to simplify the design, equation 3.25 is expressed in s-domain and will be used to derive the transfer function:

$$U_{dq}^*(s) = (R + sL)I_{dq} \tag{3.26}$$

Proportional-Integral (PI) controller is needed to control the steady state error of both current components, a simplified block diagram shown in Figure 3.8 is used to derive the transfer function and design the PI controller parameters.

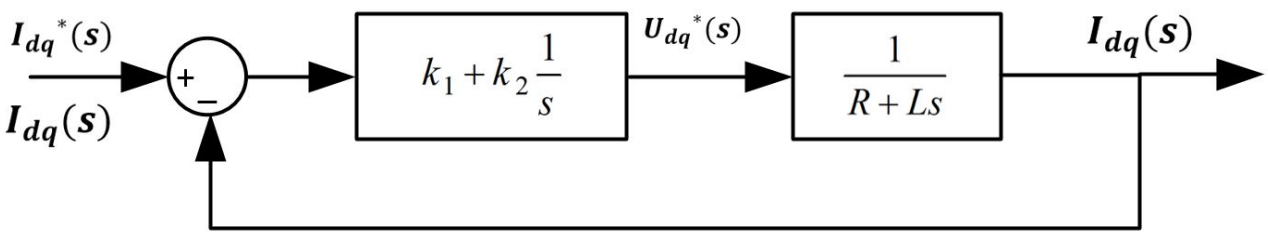

FIGURE 3.8: Closed loop linear current controller

System transfer function is defined as:

$$\frac{I_{dq}}{I^*_{dq}} = \frac{G}{1+GH} \tag{3.27}$$

Where, H is unity, and G is the open loop transfer function. By substitution of G into equation 3.27, second order transfer function is derived:

$$\frac{K_1 s + K_2}{s^2 L + (K_1 + R)s + K_2} \tag{3.28}$$

by comparing the system transfer function with general second order transfer function, K_1, and K_2 can be expressed as:

$$\begin{aligned} K_1 &= 2\zeta\omega_n L - R \\ K_2 &= \omega_n^2 L \end{aligned} \tag{3.29}$$

After some tuning of ζ, and ω_n, the PI controller parameters were chosen to be: K_1 = 0.3831 K_2 = 1.7021.

In summary, current controller is needed to be implemented on the proposed SS-MMC topology to have closed loop control on current and power under static load. The designed current controller can be modified to be applied on dynamic load for AC motor drive purposes, where the direct current component can be used to control the flux in the machine, and the quadrature component will be responsible for speed control. Simulation and discussion of the results for the current controller with SS-MMC topology under static load is conducted in Chapter 4.

3.1.8 Efficiency and Reliability

The proposed converter power losses are mainly divided into: switching losses and conduction losses. The conduction losses is the energy losses during the ON state of the MOSFET and it depends upon the amount of the drain current and the internal resistance of the MOSFET which is given by:

$$P_{c,MOS} = V_{ds} i_d = R_{ds,on} i_d^2 \tag{3.30}$$

where, V_{ds} and i_d are the drain-source voltage and the drain current of the MOSFET, respectively.

As the converter consists of n SMs in each leg, and each SM consists of four MOSFETs where two of them are turned on only if the the dead time is ignored as each two MOSFETs operate

complementary to each other. So, the leg conduction losses is $4n$ the conduction losses of single MOSFET switch. The switching losses are the energy losses caused by turning on and off the MOSFETs, and they depend on the voltage and current of the battery cells, and on the rise and fall times. Having a large number of switches in SS-MMC topology, does not mean that it has high power losses and low efficiency since no need to turn on all the switches all the time. In comparison with the two-level inverter, the switching losses and conduction losses in the SS-MMC is lower. The efficiency of the SS-MMC topology is expected to have its lowest value when it is required to turn on all the switches at the same time.

The traditional two-level inverter has 6 switches, where in all cases and for any value of the required power, they must be fully operated. The static reliability of traditional two-level inverter is given by [9]:

$$R = P^6 \tag{3.31}$$

where,
P: is the static reliability of a single switch.
R: is the reliability of the whole converter.

On the other side, in the SS-MMC converter, if any one of the switches or SM is damaged or faulted, the whole leg does not become useless, since the damaged switch or SM can be simply replaced by another one. However, during the operation of the car, the faulty SM will result in reducing the voltage level to $(n-1)$. If the maximum power required, the unbalanced voltage generated because of reducing the level of the voltage will result in reducing the reliability of the converter to zero, since all SMs and switches must be healthy in this case. Therefore, the reliability of the SS-MMC depends upon the required power. As the range of the power required is from $\frac{(k-1)P_n}{n}$ to $\frac{(k)P_n}{n}$, where P_n is the nominal output power of the converter. Therefore, the converter must have at least k SMs healthy in the leg and the switches of each SM must be healthy. The static reliability of the SS-MMC is given by [9]:

$$R = \Big(\sum_{i=k}^{n} \binom{n}{i} (P^4)^i (1-P^4)^{n-i} \Big)^3 \tag{3.32}$$

As a comparison, the reliability against required power in the two-level and SS-MMC inverters with a single switch (MOSFET) reliability of p=0.9, and p=0.99 is drawn in Figure 3.9:

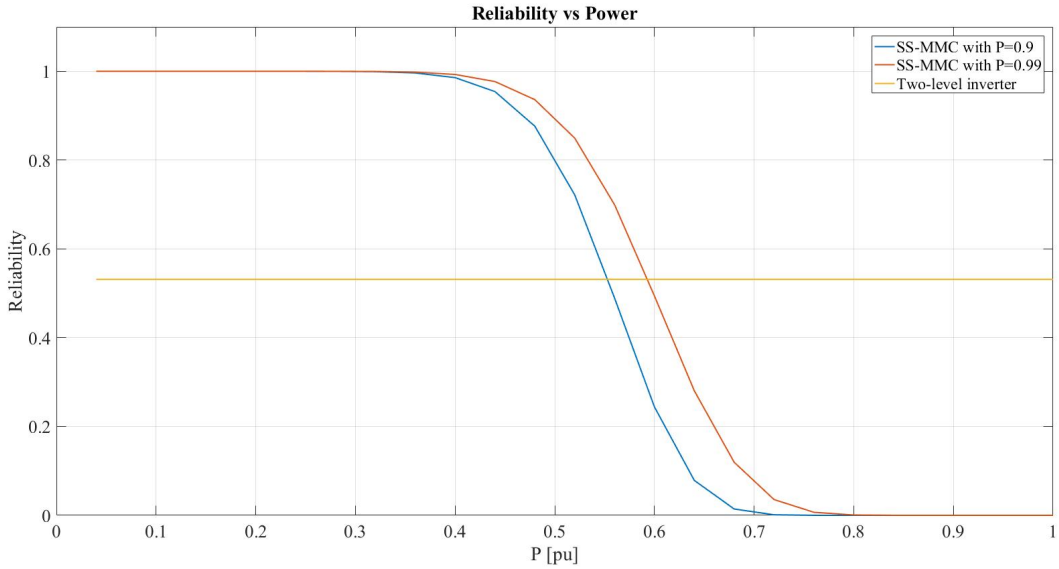

FIGURE 3.9: The reliability of two-level and SS-MMC converters for p = 0.9 and p=0.99

As a result, the MOSFETs must be chosen carefully with proper reliability to improve the overall reliability in MMC topologies.

Chapter 4

Simulation Results

This chapter illustrates simulation outputs for variable stages of the system obtained using MATLAB Simulink. The simulation outputs are arranged in a manner presenting a stage by stage operation validation of the system. It will show the output of the converter under no load with different numbers of SMs and under static load with open loop control. The voltages of each leg/phase and the line voltages and currents of the converter will be presented. The total harmonic distortion (THD) of the line voltages and line currents will be presented and discussed. The voltage balancing of the capacitors of each leg and between the three legs will be shown and discussed. This chapter also shows the operation of the proposed converter under static load conditions with a decoupled dq current controller.

4.1 Bidirectional Boost Converter Simulation

In this section, the bidirectional boost converter will be tested under a resistive load of 20Ω, with an inductor value of 1mH, a capacitor value of 50mF, an input voltage of 3.7V, a switching frequency of 2kHz, and with different duty cycle values. The values of passive elements C, and L were chosen based on the required ripples in the voltage and current. Where, the voltage ripple depends on output current, switching frequency, and capacitor value, while the current ripple depends on the duty cycle, switching frequency, input voltage, and inductance value. The MATLAB circuit is shown in Figure 4.1.

Gate signals of the two switches of the converter are shown in Figure 4.2, with a duty cycle of 50%, the two signals are opposite to each other with ignoring the dead time.

Output voltages are shown with varying the duty cycle, the average voltage increases with increasing the duty cycle. From input current results, shown in Figure 4.6 and Figure 4.7, it is concluded that the usage of bidirectional boost converter with suitable values of the input inductor, duty cycle, and switching frequency can provide positive and continuous current, which is more healthy for the battery cells.

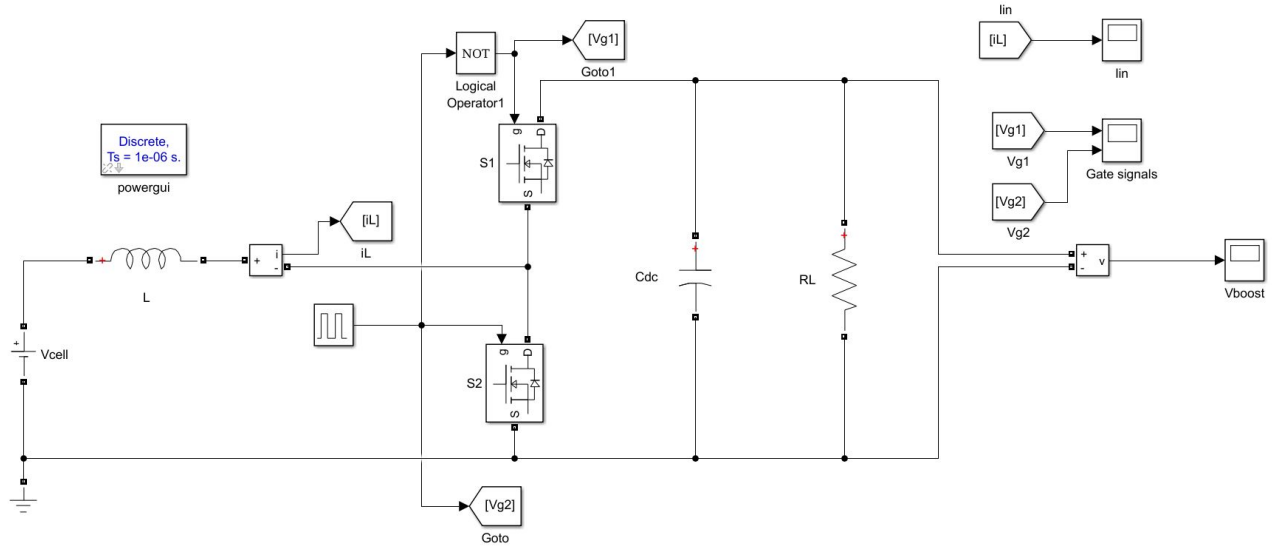

FIGURE 4.1: Bidirectional boost converter MATLAB model

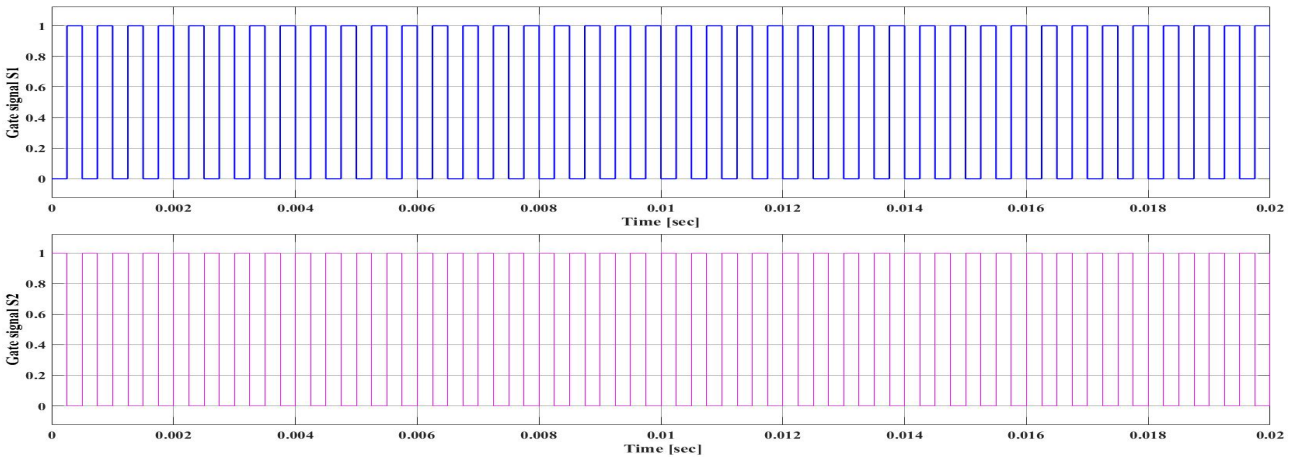

FIGURE 4.2: Bidirectional boost converter gate signals

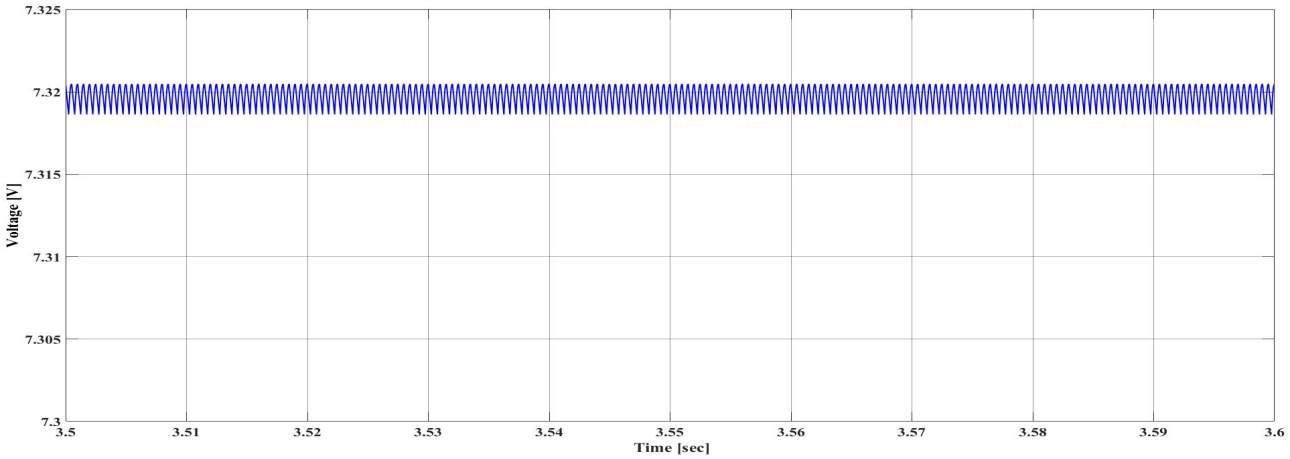

FIGURE 4.3: Bidirectional boost converter output voltage at D=0.5

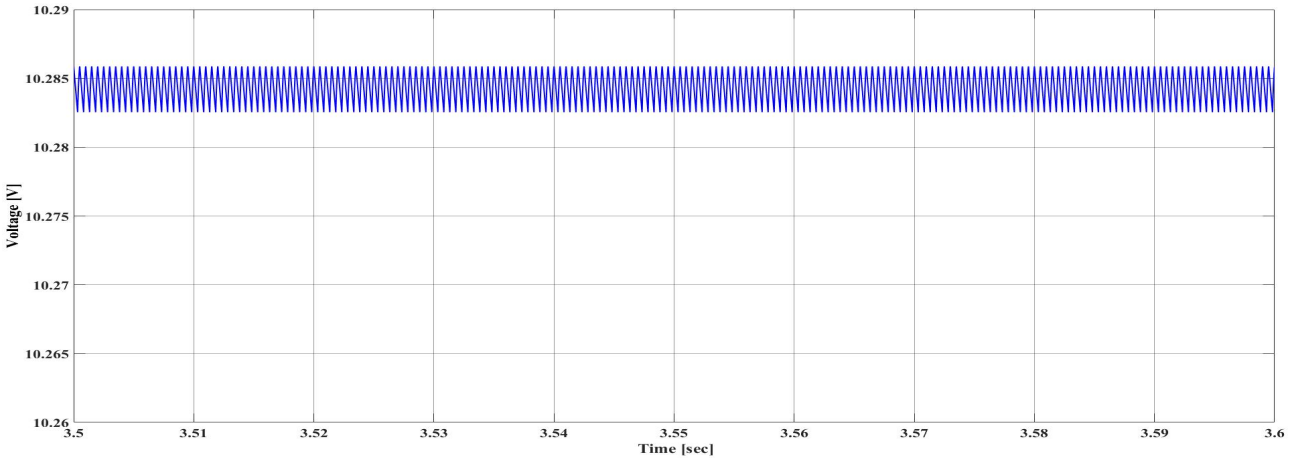

FIGURE 4.4: Bidirectional boost converter output voltage at D=0.65

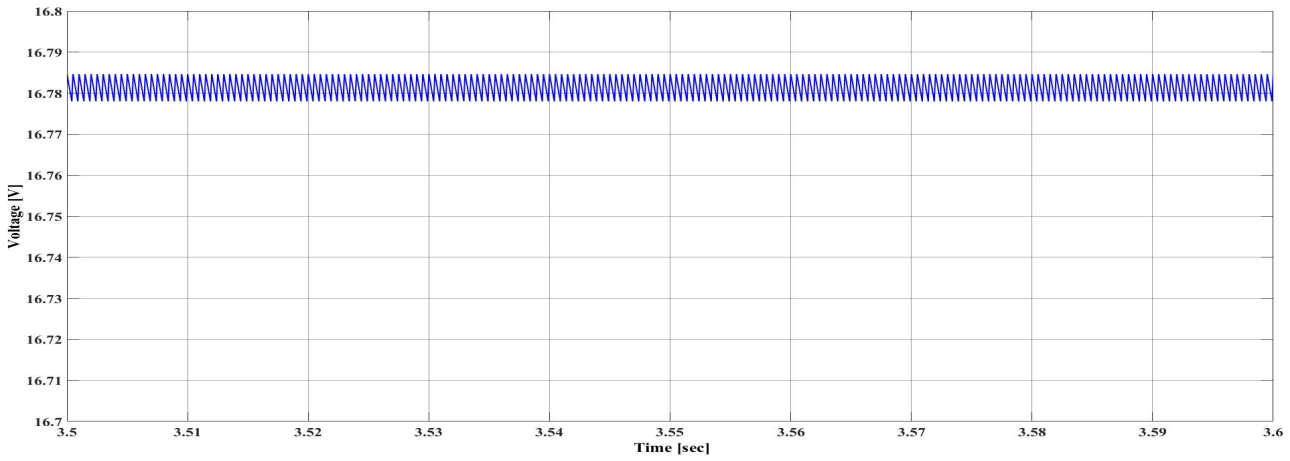

FIGURE 4.5: Bidirectional boost converter output voltage at D=0.8

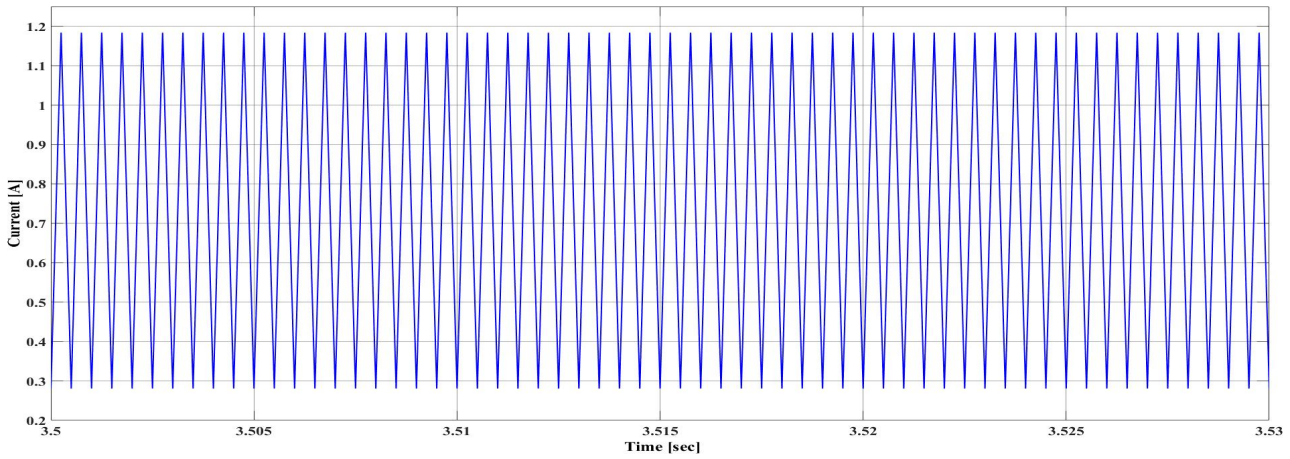

FIGURE 4.6: Bidirectional boost converter input current at D=0.5

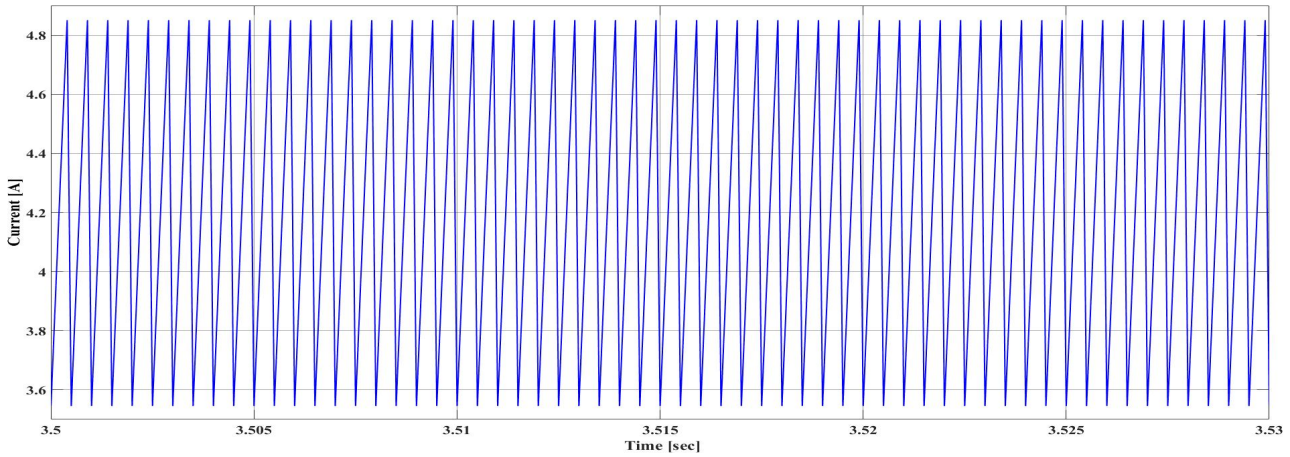

FIGURE 4.7: Bidirectional boost converter input current at D=0.8

4.2 SS-MMC Simulation Results with no Load

The system, shown in Figure 4.8 simulated under the defined simulation parameters listed in Table 4.1. In this section, the bidirectional boost and the battery cells were replaced by an ideal voltage source with a DC value adjusted according to $V_{boost} = 2 * \sqrt{2/3} * 220/(N * 1.155)$.

In order to study the relationship between the number of SMs and the THD under the constraint of having constant line-line voltages, the system is simulated under different number of SMs (N = 2, 4, 6,..., 25), and the results were as follow:

TABLE 4.1: Simulation defined parameters with no load

Parameter	Value
Buck Switching frequency f_{s1}	5 KHz
Fundamental frequency f_1	50 Hz
Modulation Index M	1.155

The Figures 4.9 to 4.19 show the output line-line voltages at different number of SMs. As the number of SMs increases, the voltages waves become more closer to the sinusoidal with less harmonic contents. Figure 4.20 summarizes the effect of changing the number of SMs on the THD percentage, as the number of levels on the output voltage increases, the THD will decrease. It is noticed also, as the number of SMs becomes large, the effect on the THD becomes less significant.

In Figure 4.21, the frequency and modulation index were changed in the same ratio in order to verify proper operation under constant v/f control. It emphasizes also on the concept of decreasing the THD with the increasing of modulation index.

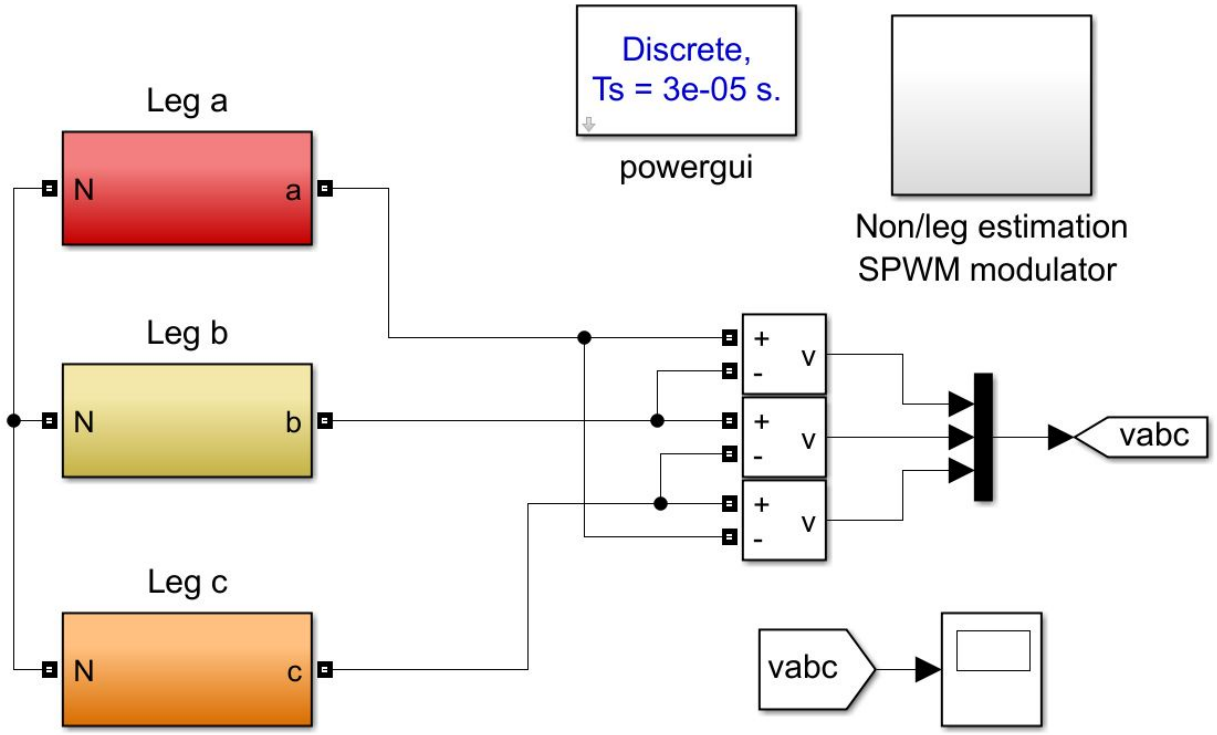

FIGURE 4.8: SS-MMC with no load

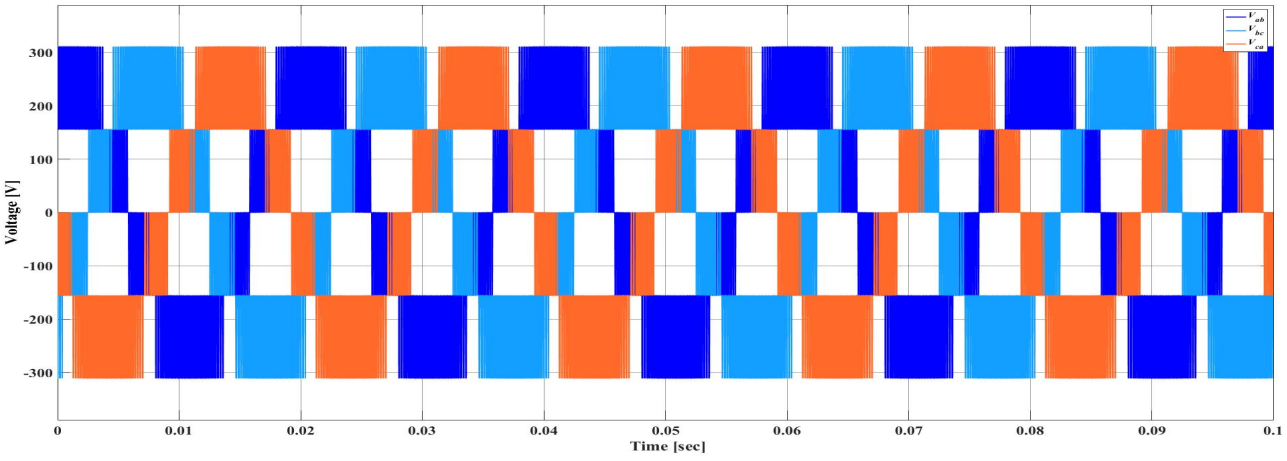

FIGURE 4.9: Line to line voltages for N=2

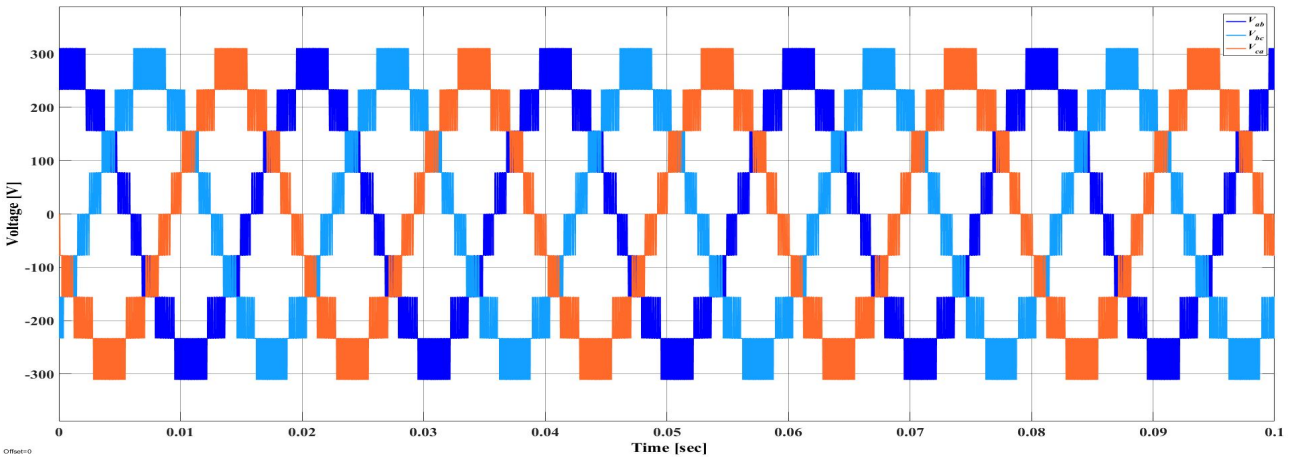

FIGURE 4.10: Line to line voltages for N=4

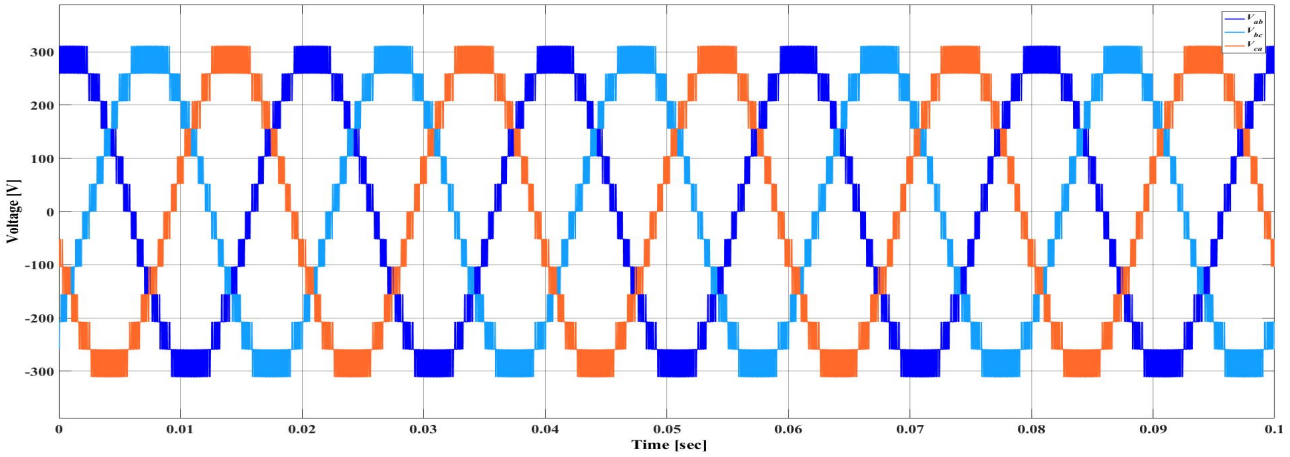

FIGURE 4.11: Line to line voltages for N=6

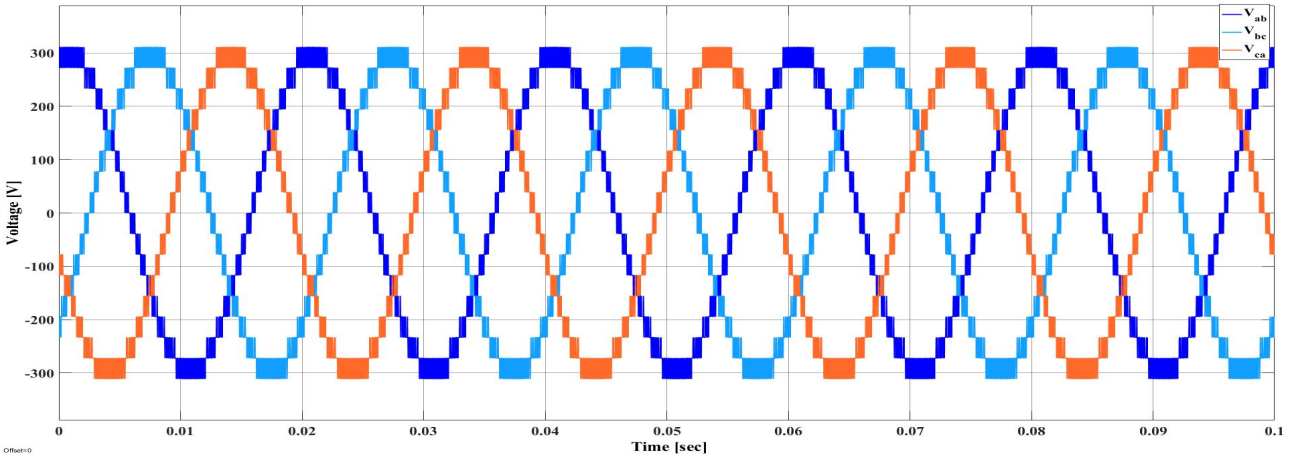

FIGURE 4.12: Line to line voltages for N=8

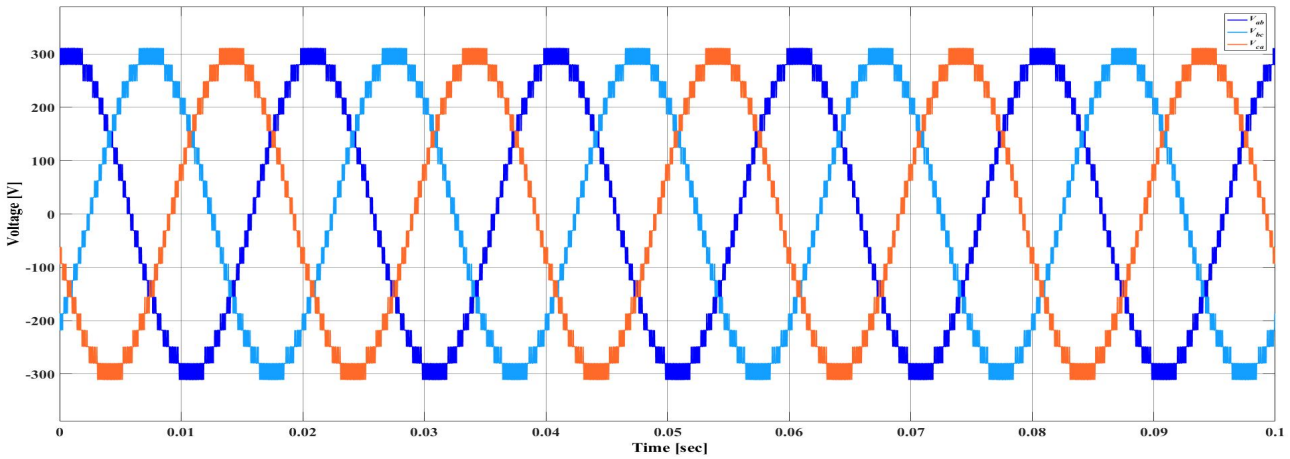

FIGURE 4.13: Line to line voltages for N=10

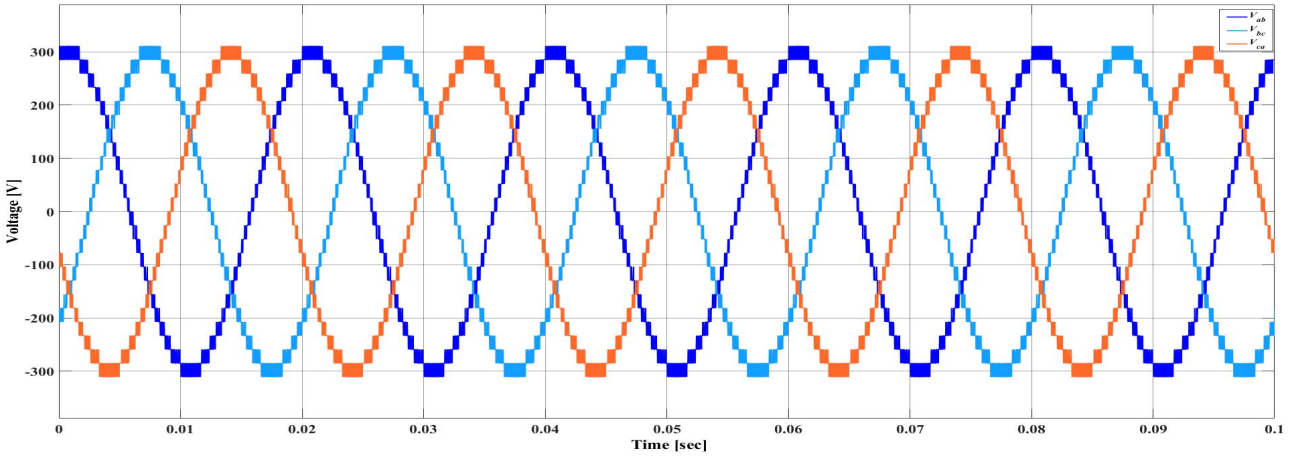

FIGURE 4.14: Line to line voltages for N=12

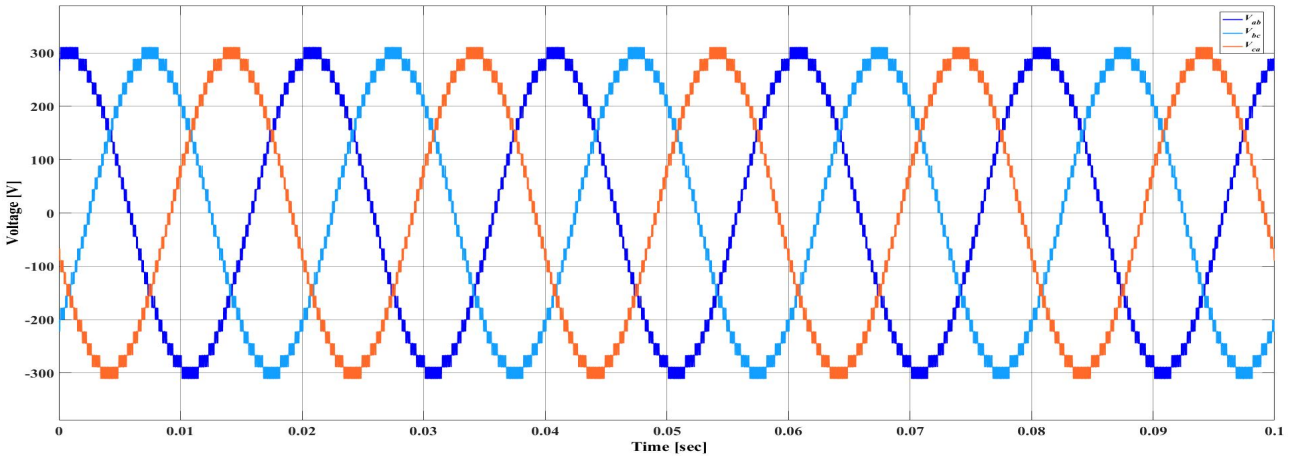

FIGURE 4.15: Line to line voltages for N=14

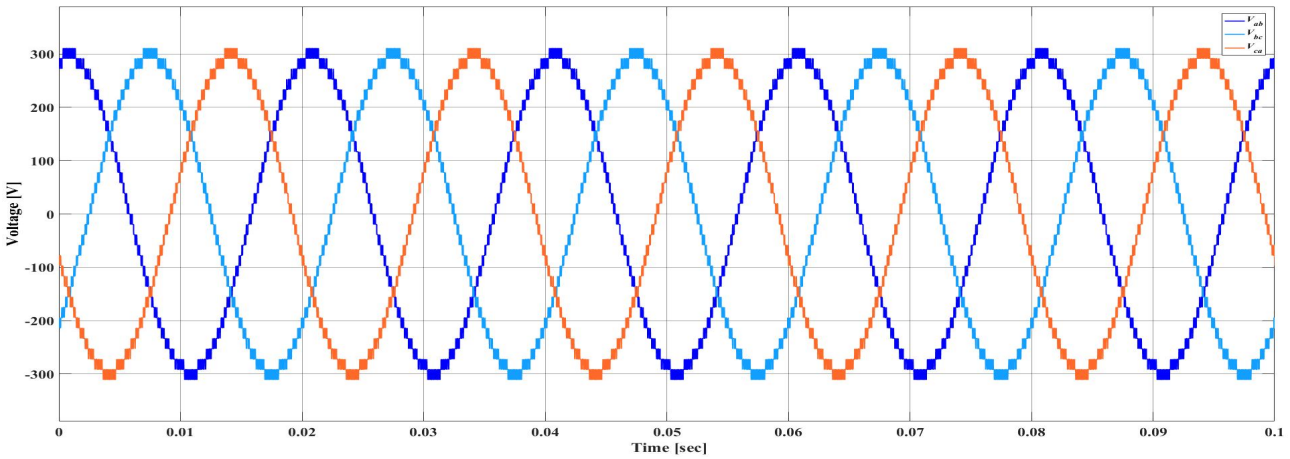

FIGURE 4.16: Line to line voltages for N=16

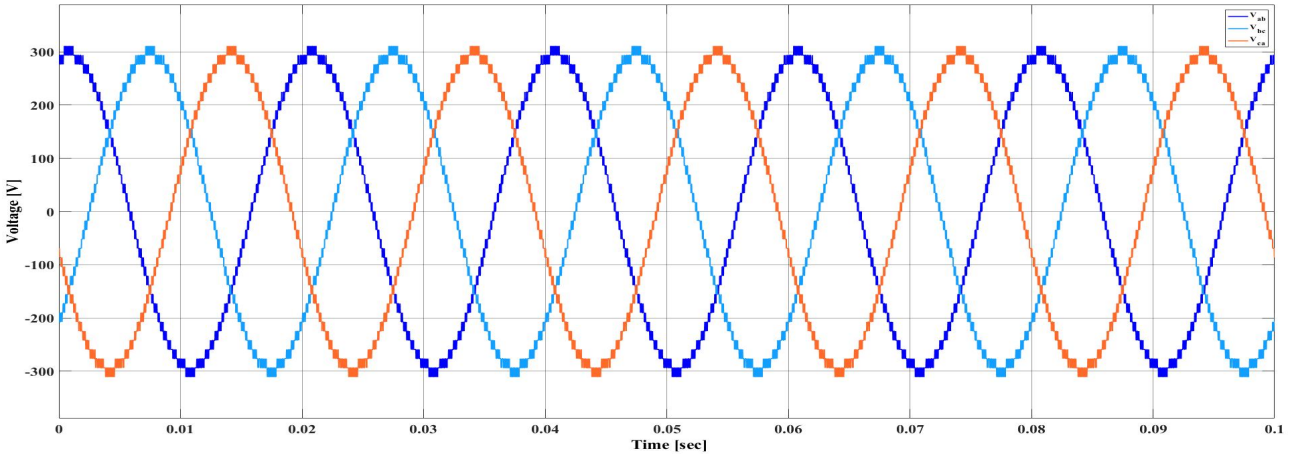

FIGURE 4.17: Line to line voltages for N=18

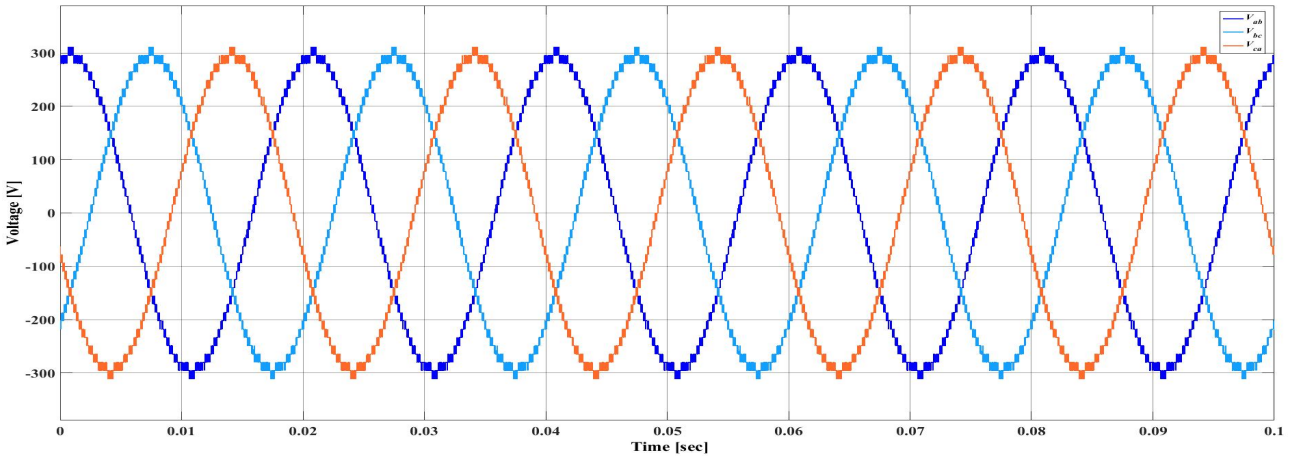

FIGURE 4.18: Line to line voltages for N=20

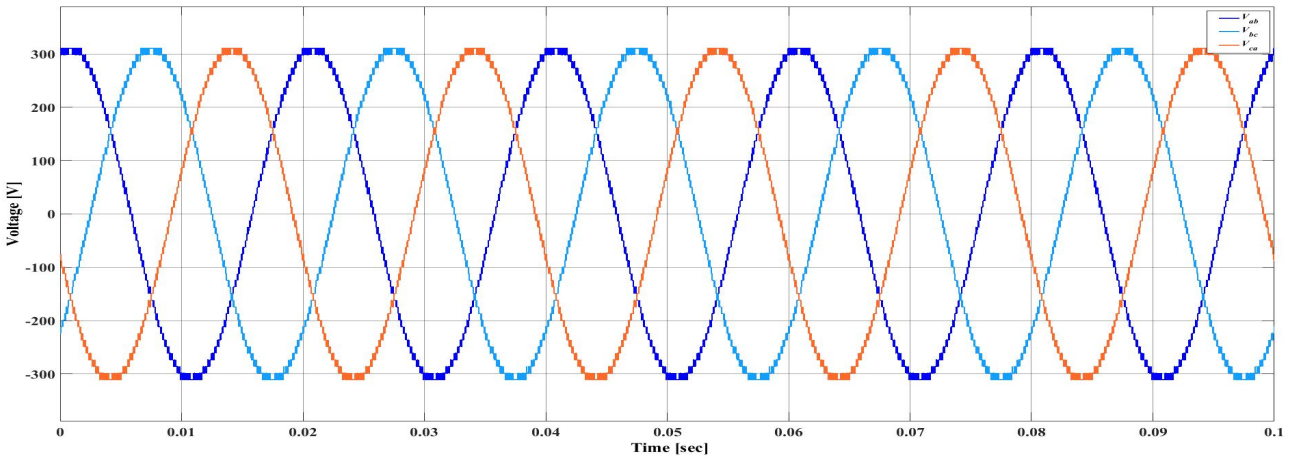

FIGURE 4.19: Line to line voltages for N=25

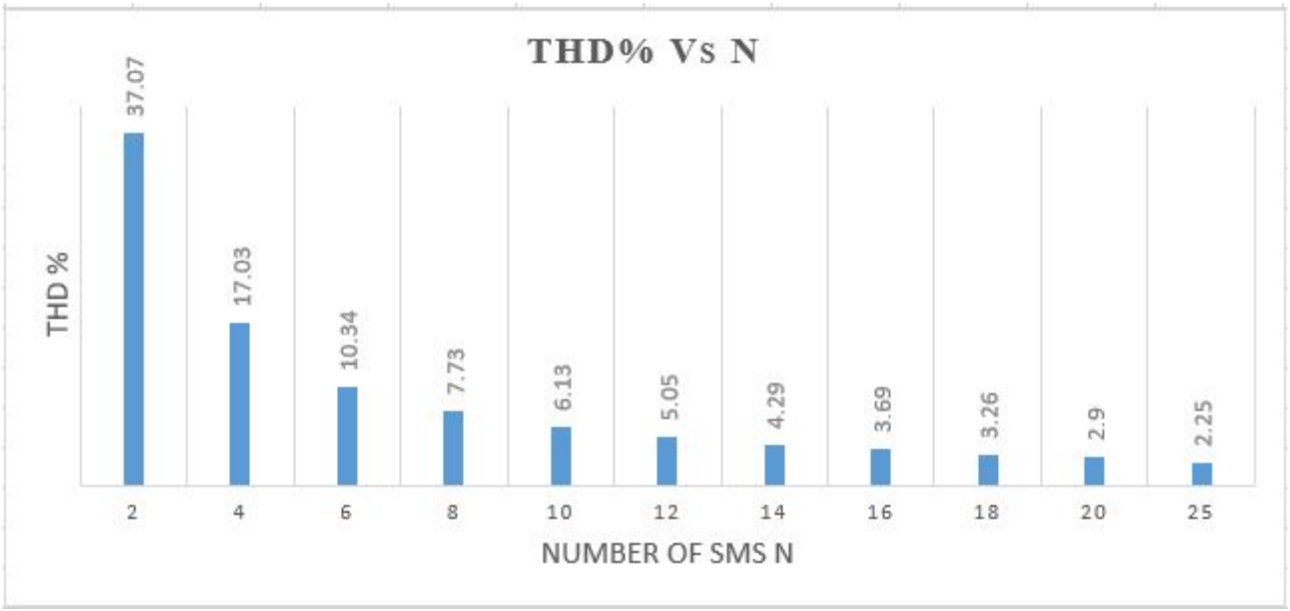

FIGURE 4.20: THD percentages of line-line voltages with different number of N

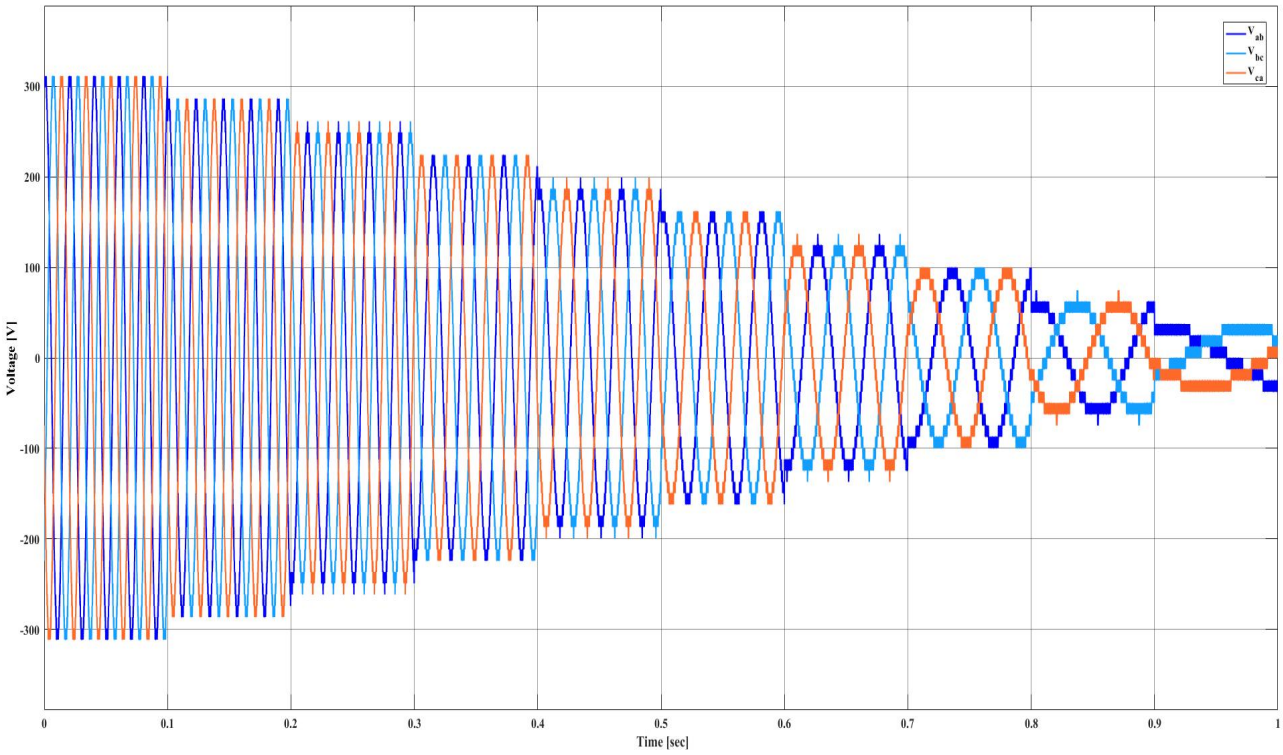

FIGURE 4.21: Line to line voltages with different frequencies and modulation indices

4.3 SS-MMC Simulation Results with Static Load and Capacitor Voltage Balancing

4.3.1 Static Load with Rated Power

In order to study the performance of the proposed converter with a static load, the circuit shown in Figure 4.22 was simulated with the simulation parameters listed in Table 4.2. For simulation purposes, the cell voltage is chosen to be constant and equals 3.7V. The switching frequency of the buck and boost converter is reduced to 2kHz, which helps in decreasing the losses in the converter. The duty cycle is determined based on this equation $D = 1 - (V_{cell}/V_{boost})$ which depends on capacitor voltage and cell voltage. In order to reach the required line-line output voltage, twenty five SMs were implemented in each leg.

The line-neutral voltages shown in Figure 4.23, oscillate between 0 and nV_{boost}, where V_{boost} is the output voltage at the SM capacitor. They have three main components: the fundamental components, a DC component, and the injected third-harmonic component. However, the DC and the third harmonic components were eliminated in the line-line voltages as shown in Figure 4.24, which makes it necessary to connect the motor terminals in Wye configuration and isolate its neutral point from converter neutral.

From Figure 4.25 it is clear that the resulted currents are purely sinusoids with zero DC components, due to multilevel converter, which means that there is no need for external filtering, and it can provide smooth torque with high efficiency.

In Figure 4.26 it is clear that the cell current is continuous, positive, and balanced, since the capacitors' voltages are balanced, which help in increasing the lifetime of the battery cells. However, it has two types of ripples; one from the switching, and the other is related to the

TABLE 4.2: Simulation defined parameters with static load

Parameter	Value
Nominal cell voltage	3.7V
Buck Switching frequency f_{s1}	2 kHz
Boost Switching frequency f_{s2}	2 kHz
Fundamental frequency f_1	50 Hz
Modulation Index M	1.155
Number of SMs N	25
Motor real Power P_r	45 KW
Power Factor PF	0.9
Inductor value L	3 mH
Capacitor value C	400 mF
Duty cycle D	0.7026

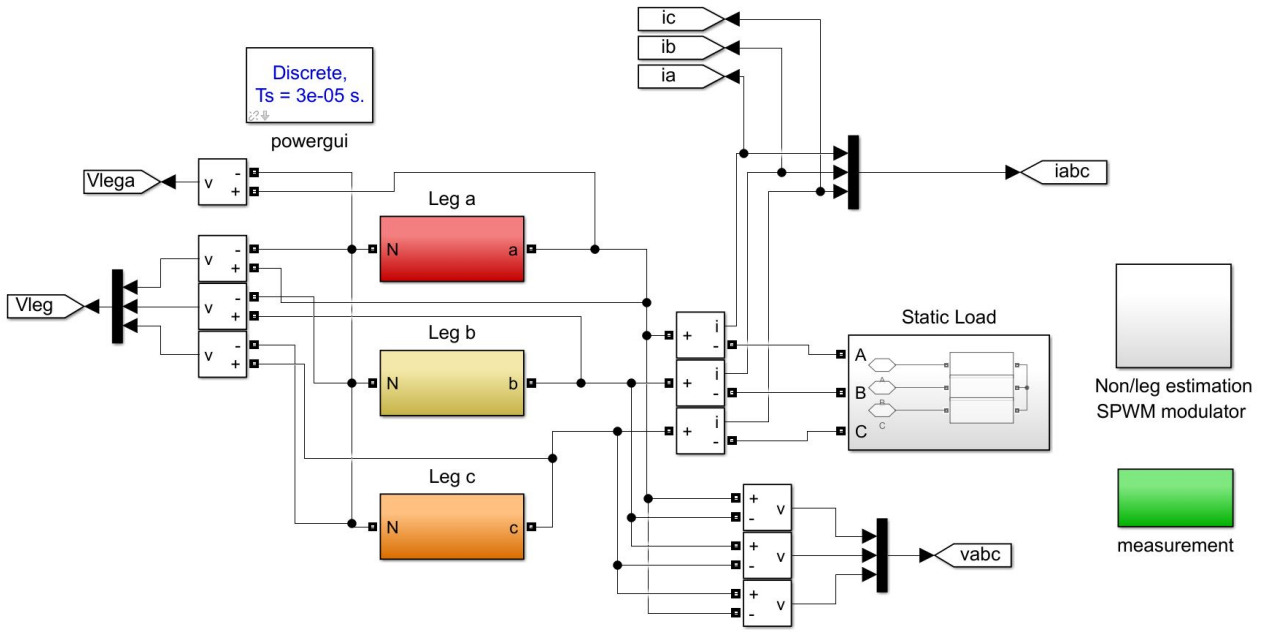

FIGURE 4.22: SS-MMC with a static load

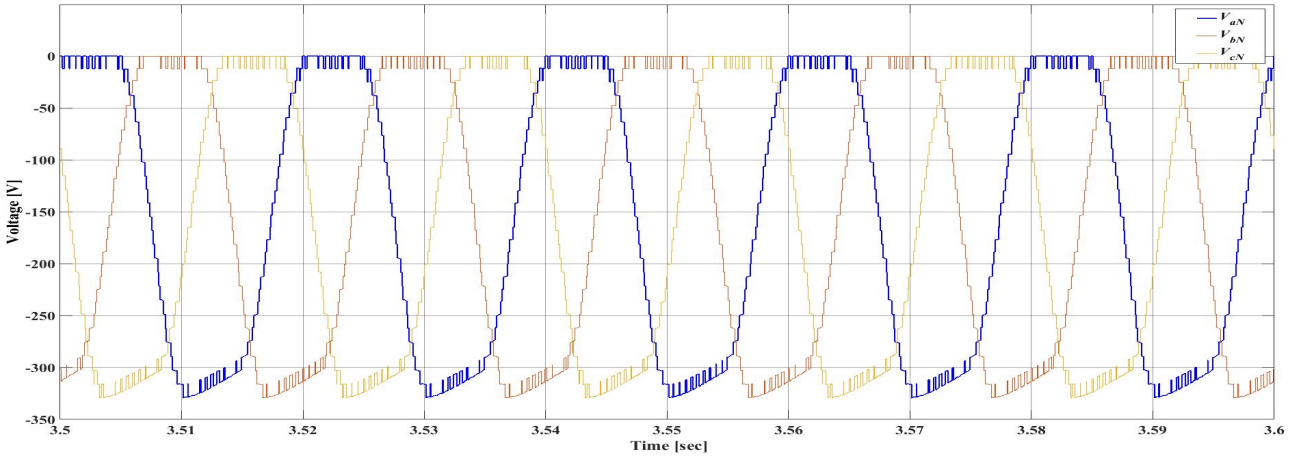

FIGURE 4.23: Line to neutral voltages $[V_{aN}, V_{bN}, V_{cN}]$

capacitor voltage ripple and it is the most significant one, as having high current ripple may cause discontinuity in the current and decrease the efficiency and the lifetime of the battery cells. Figure 4.27 shows balancing of the the voltages at the output capacitors of the SMs in each leg. The average output voltage equals to 12.44V, while the peak to peak value is around 1.5V which can be decreased by using higher values of the output capacitors.

In order to validate the balancing at the output voltages of the capacitors with the usage of real batteries which may have different cells voltages occurring in the range between 3.7V-4.2V, different cells voltages used as inputs to the SMs and the output capacitors' voltages are checked as shown in Figure 4.28. The duty cycle of the converter changes based on input cell voltage to keep the capacitors' voltages balanced.

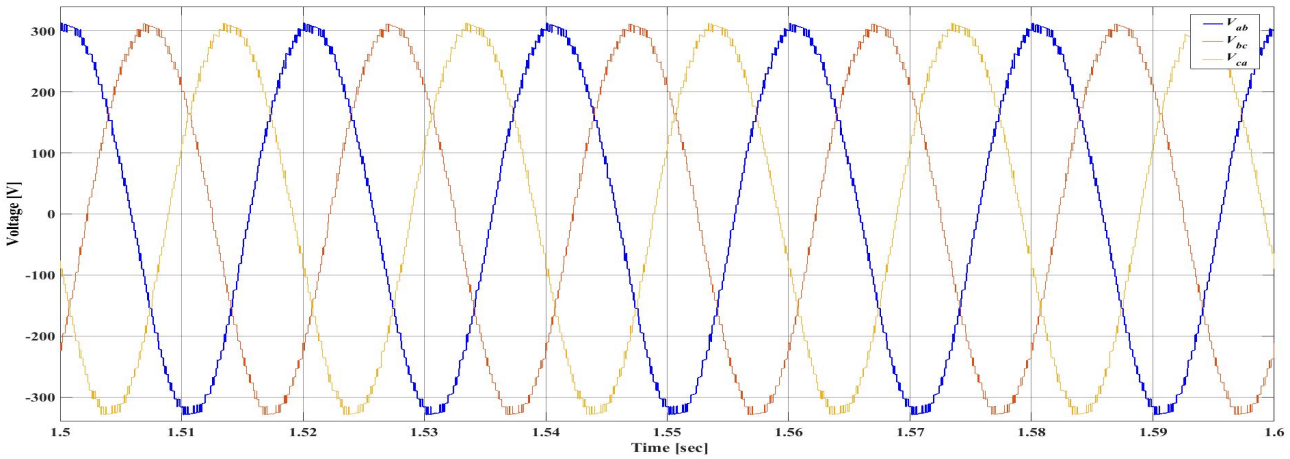

FIGURE 4.24: Line to line voltages $[V_{ab}, V_{bc}, V_{ca}]$

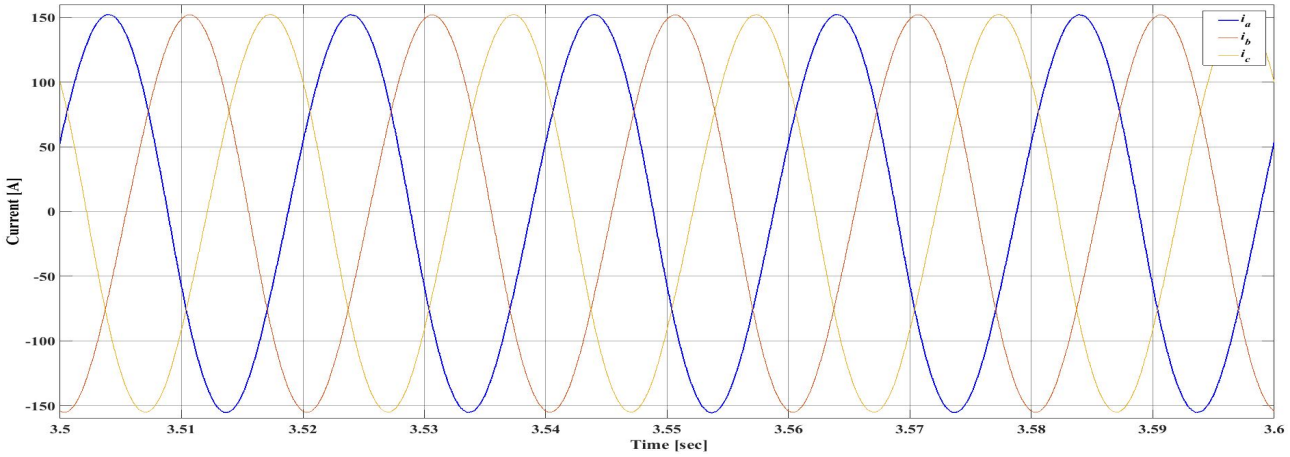

FIGURE 4.25: Lines-currents $[i_a, i_b, i_c]$

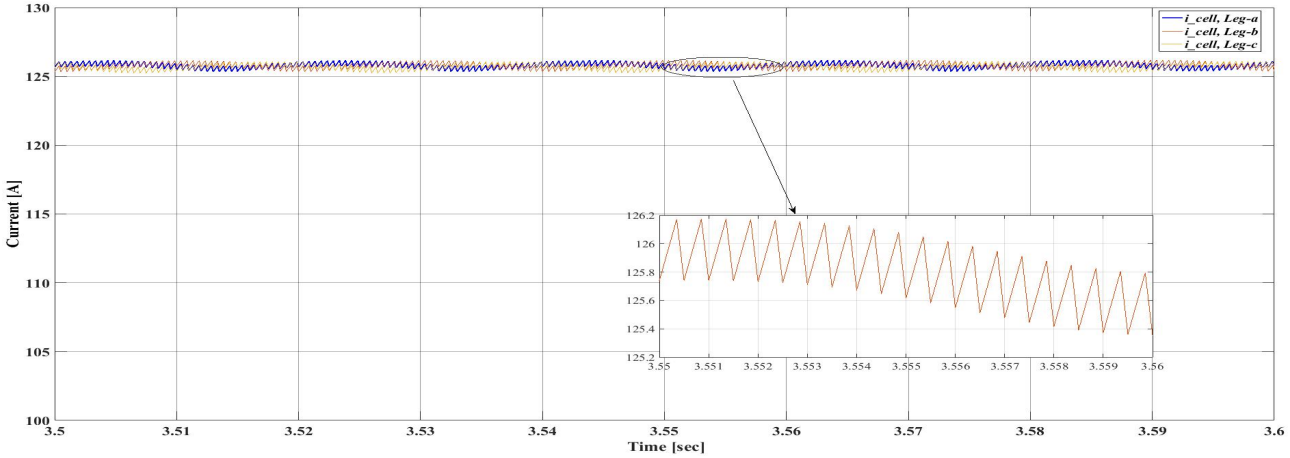

FIGURE 4.26: Input currents of the Battery Cells

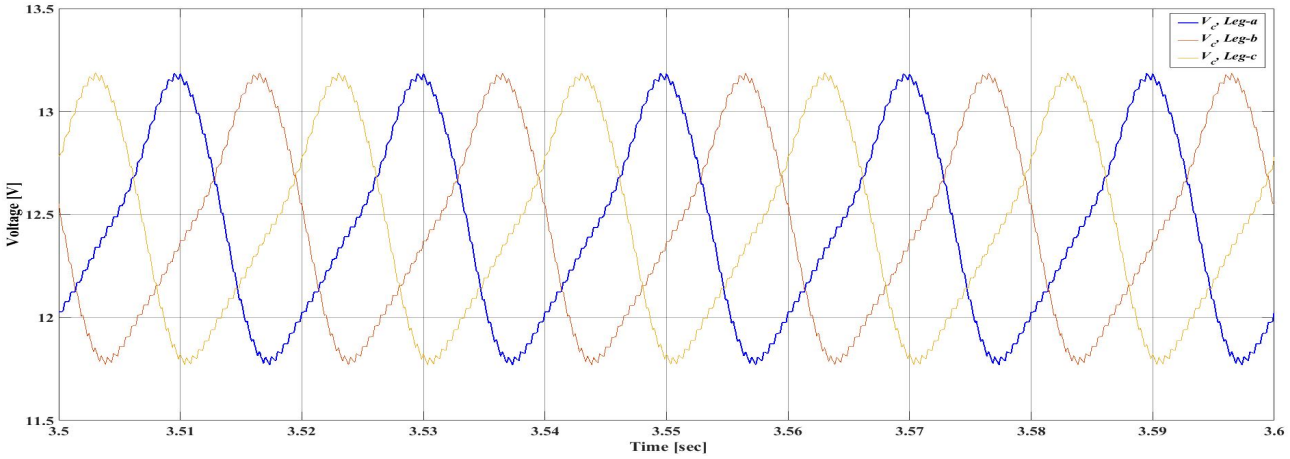

FIGURE 4.27: Voltages across capacitors of each leg

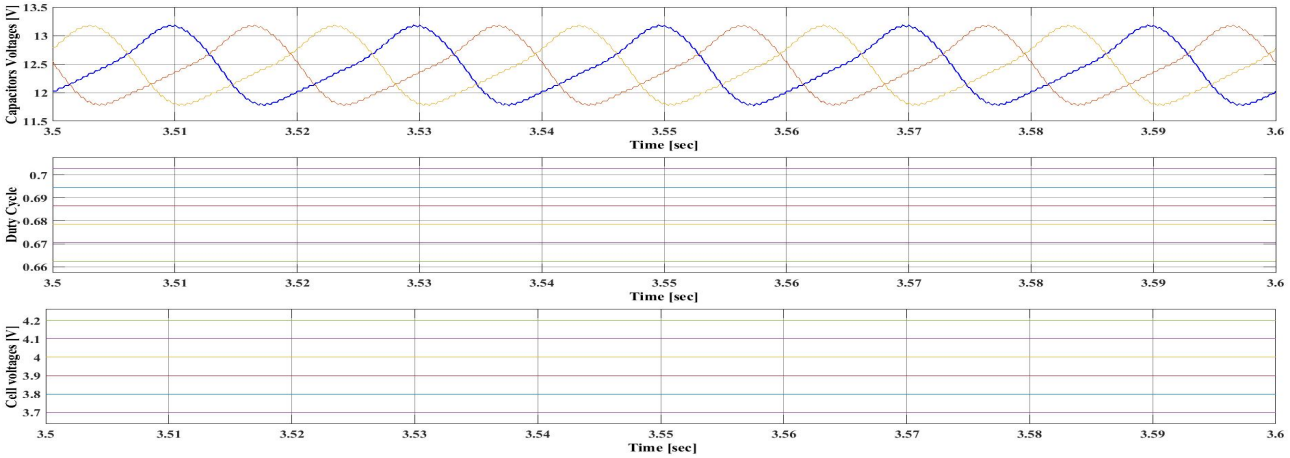

FIGURE 4.28: Capacitors voltages balance with different cells voltages

4.3.2 Static Load Power Change Effect

In this section the static load power was decreased to 25kW, while the other simulation parameters are kept as in Table 4.2, and the figures 4.29 to 4.32 were obtained:

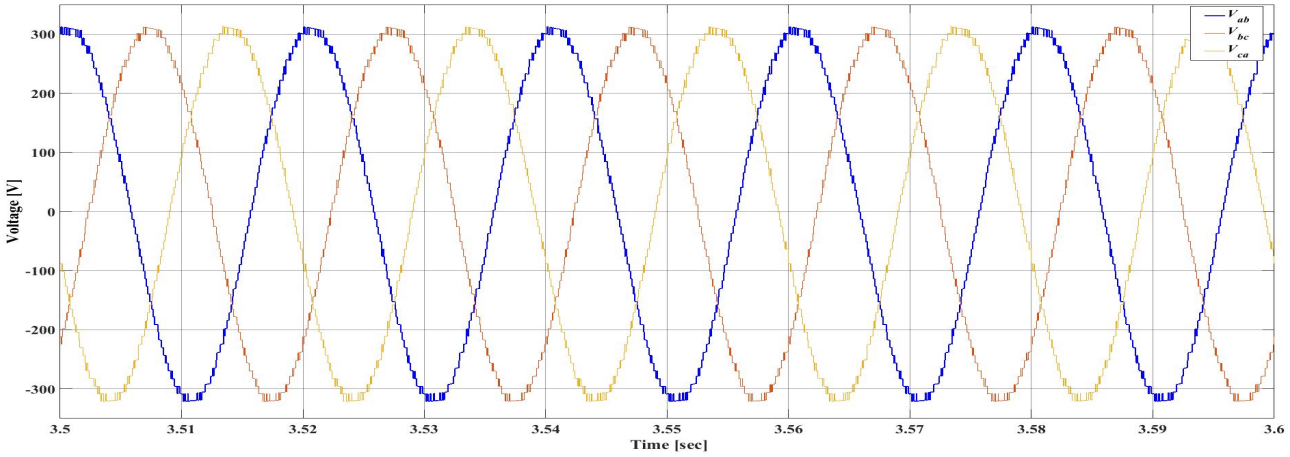

FIGURE 4.29: Line to line voltages $[V_{ab}, V_{bc}, V_{ca}]$

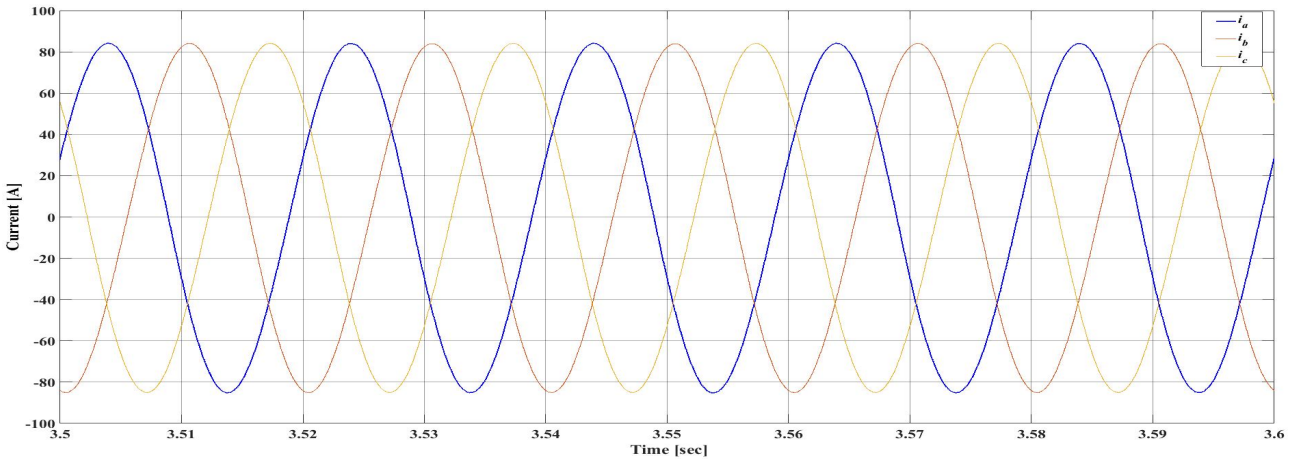

FIGURE 4.30: Lines-currents $[i_a, i_b, i_c]$

From the results shown in the aforementioned figures, it could be concluded that when the power is decreased, the steady state line currents are decreased with same ratio compared to line currents at nominal power. The peak to peak capacitors ripple is also decreased to 0.75V, thus the current ripple on the input current also decreased.

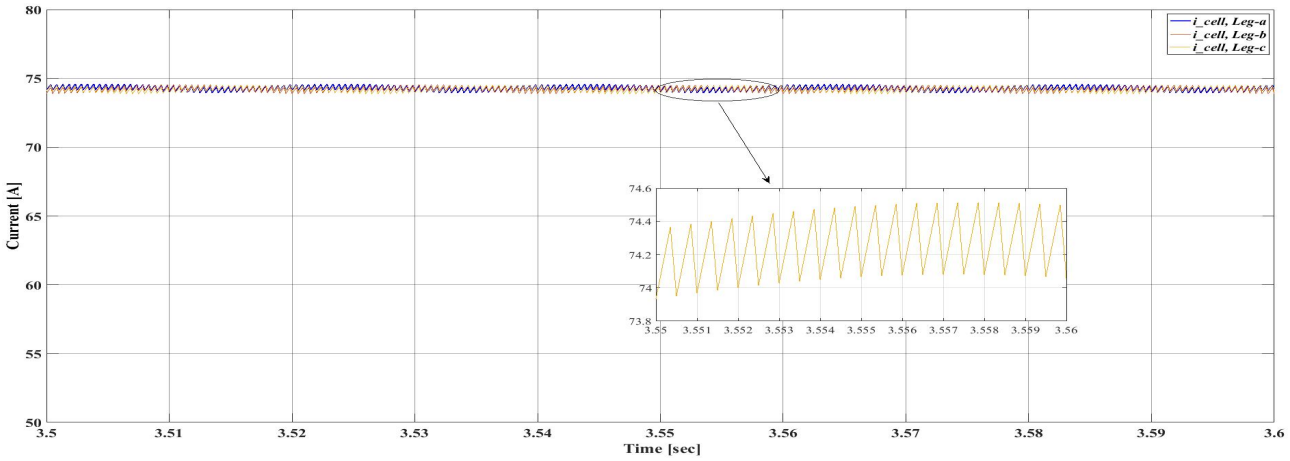

FIGURE 4.31: Input currents of the Battery Cells with half power

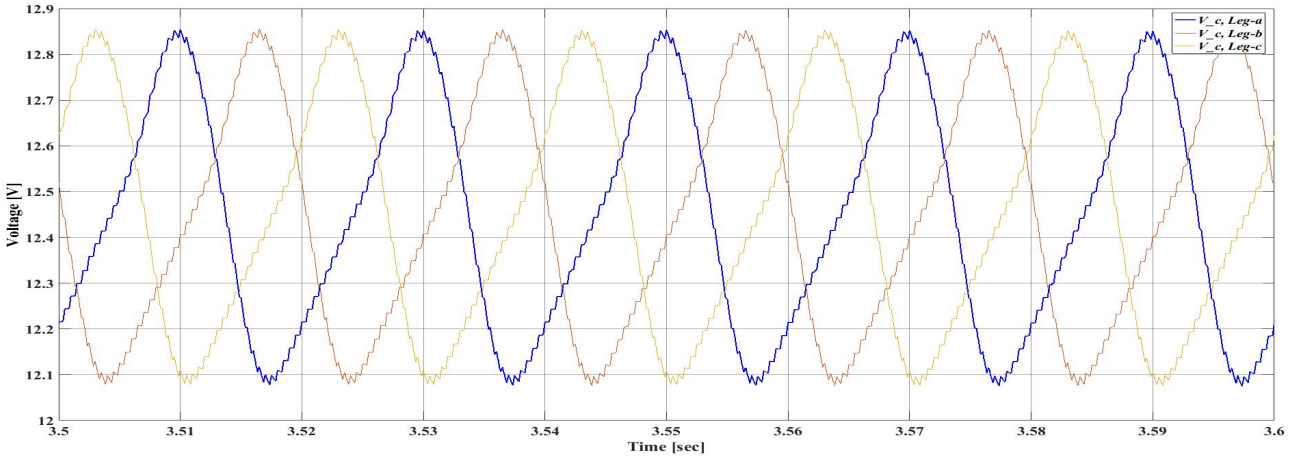

FIGURE 4.32: Voltages across capacitors of each leg

4.3.3 The Effect of Changing Load Frequency

The simulation of this part done on the same model with changing the fundamental frequency to half its value 25Hz, and the modulation index to 0.5775, while the remaining simulation parameters were kept as in Table 4.2. The results of this section give an indication that the proposed converter can be used with V/f control for AC motor drive.

From the results it is noticed that the line-line voltage and line currents decreased to its half value, while the voltage ripple on the capacitors' voltages increased to around 1.5V, hence the current ripple in the input current increased. So the design of the capacitor in the practical implementation should depend on the smallest frequency and nominal current.

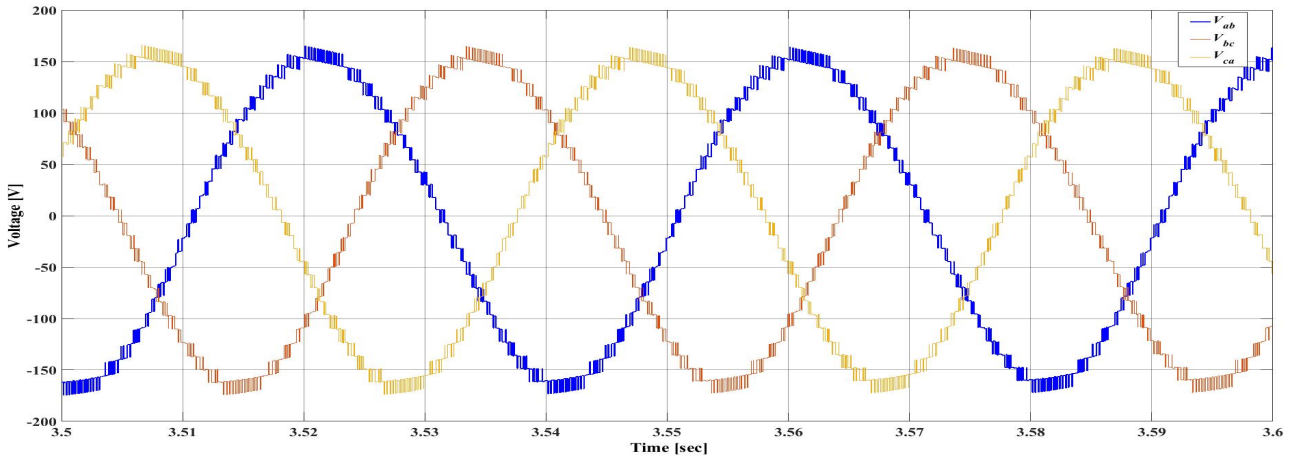

FIGURE 4.33: Line to line voltages $[V_{ab}, V_{bc}, V_{ca}]$

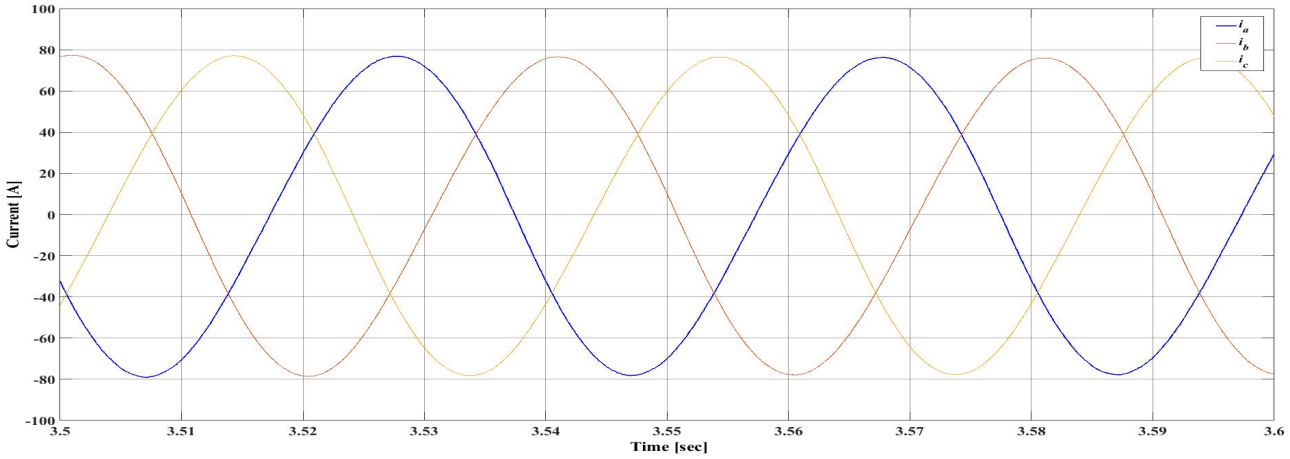

FIGURE 4.34: Lines-currents $[i_a, i_b, i_c]$

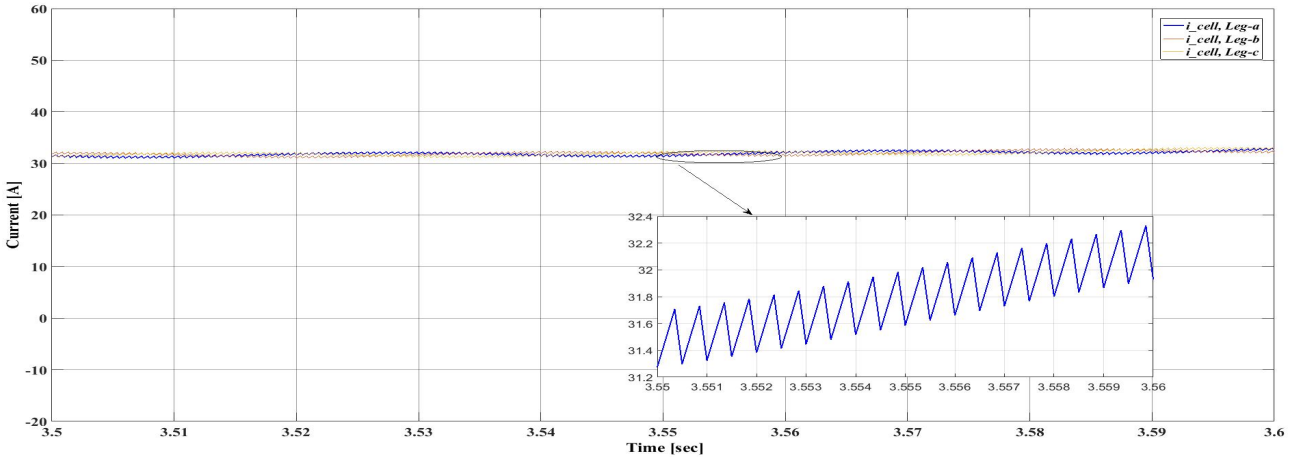

FIGURE 4.35: Input currents of the Battery Cells

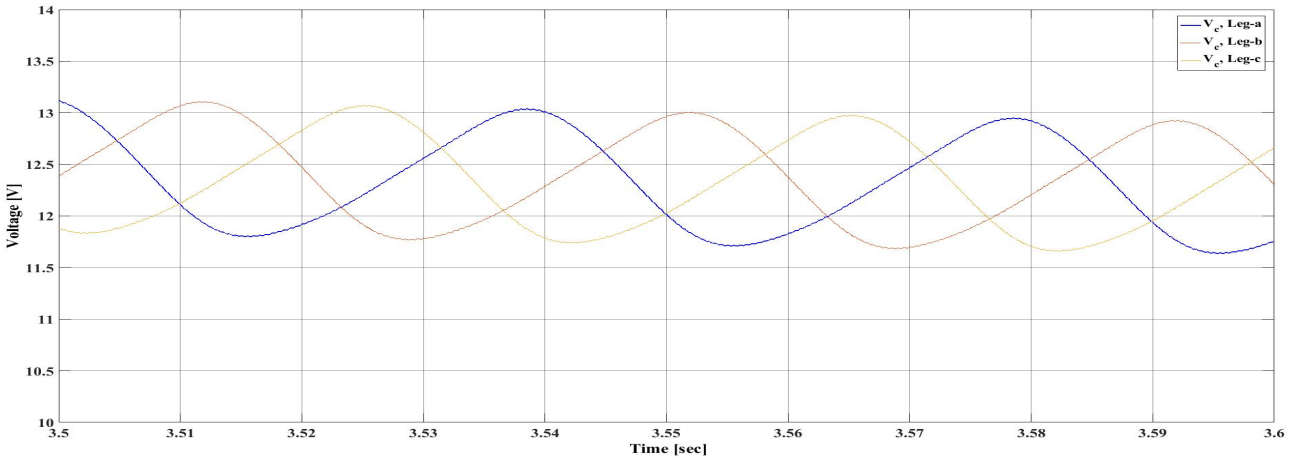

FIGURE 4.36: Voltages across capacitors of each leg

4.4 SS-MMC with Static Load and Current Control

This section intends to simulate static load with closed loop current control to prove the feasibility of the proposed topology to drive an AC motor by monitoring the current and power. The system was tested under the parameters specified in Table 4.3. The circuit is shown in Figure 4.37, and the simulation models and blocks shown in appendix A.

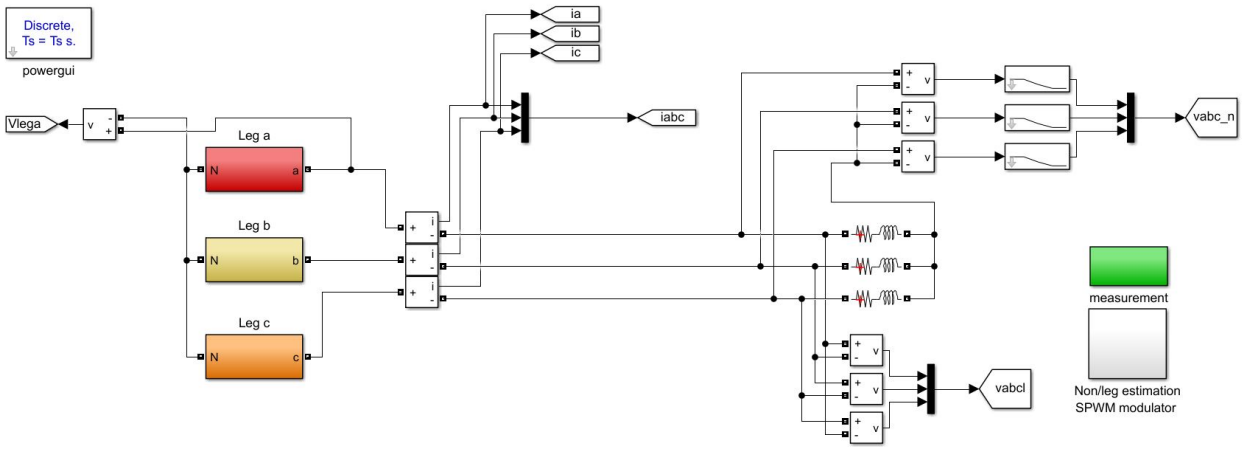

FIGURE 4.37: SS-MMC Simulink model with static load and current control

TABLE 4.3: Simulation defined parameters with static load and current control

Parameter	Value
Nominal cell voltage	3.7V
Buck Switching frequency f_{s1}	5 kHz
Boost Switching frequency f_{s2}	5 kHz
Fundamental frequency f_1	50 Hz
Nominal voltage V_n	220V
Number of SMs N	25
Real Power P	40 kW
Reactive power Q	24.790 kVAR
Nominal current In	175A
Load inductance value L_{Load}	1.7 mH
Load resistance value R_{Load}	0.8742 Ω
Power Factor PF	0.85
Inductor value L	3 mH
Capacitor value C	200 mF
Duty cycle D	0.7026

Figure 4.38 shows the direct and quadrature current components under step variations of load current (0.5pu - 1.0pu - 0.75pu - 0.25pu on the current base of 175A). With a suitable design and tuning of PI-controllers, the two current components stability was achieved as it is clear that the currents are tracking their reference values with having some transient oscillations at the starting of each step change. The results in Figure 4.39 shows that the current controller can control the real and reactive power. It is clear that the power values are proportional to the load current, when the current is set to its rated value in the period [10-20] secs, the power reaches its nominal value.

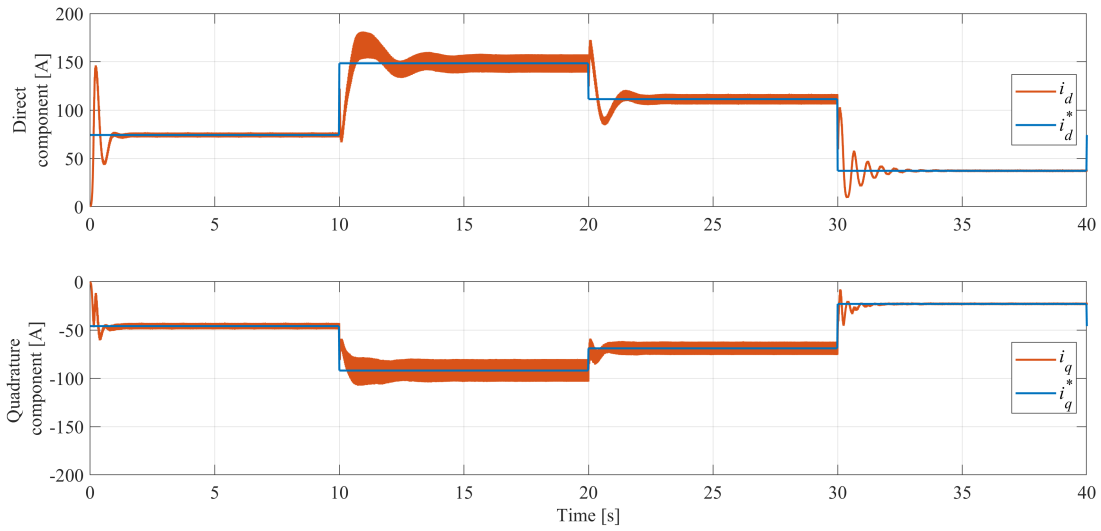

FIGURE 4.38: d-q axis current components

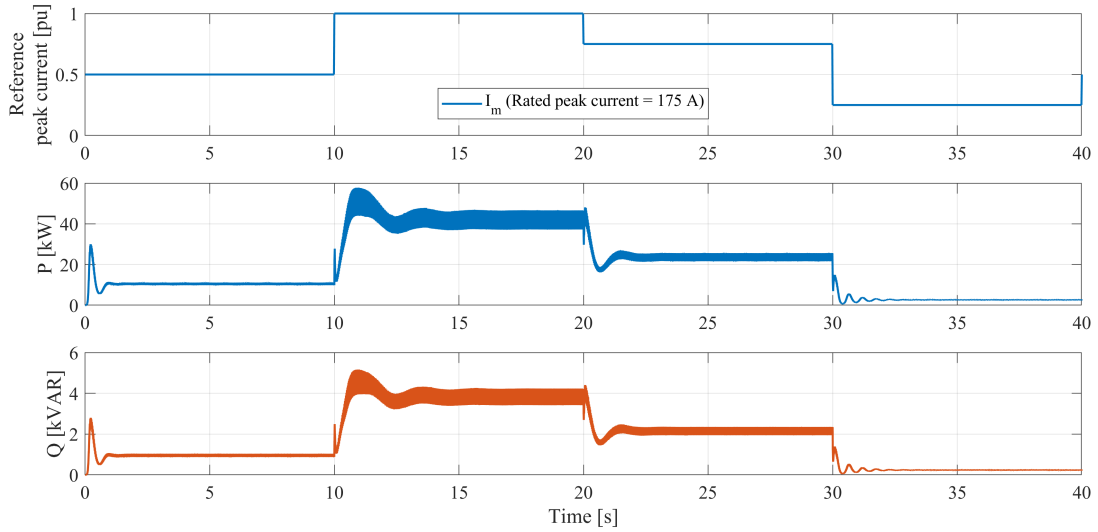

FIGURE 4.39: Real and reactive output power

In figure 4.40 the voltage across the capacitors along the whole period under the load current variations is shown. The voltages balance at each leg still present. It is concluded also that the capacitors' voltages ripple is proportional to the load current value since the frequency is fixed, as the current value increases, the ripple on the capacitors' voltages increases, and the highest ripple value will be at the rated current.

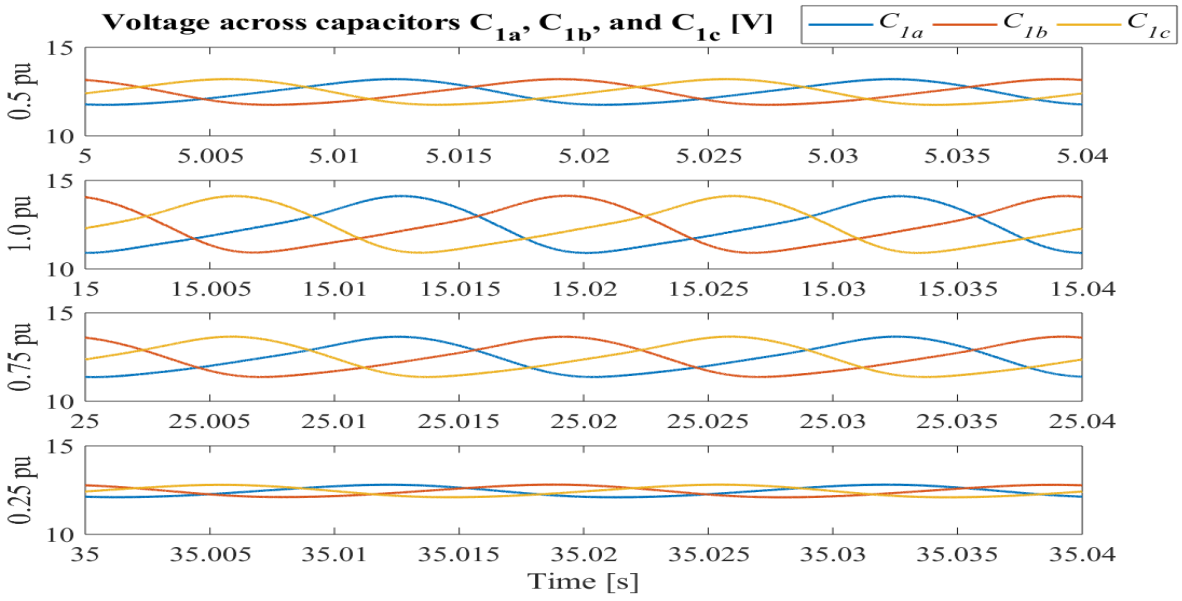

FIGURE 4.40: Voltage across capacitors

The line-line output voltages is shown in figure 4.41. The modulation index will change in proportional to the required output current (power). Therefore, the modulation index and the phase angles of the modulating waves will change via the designed current controller to provide the appropriate gate signals for the switches. When the current decreases, the

number of active SMs decreases to reach the required output voltage. Figure 4.26 shows the cell's current continuity and stability along the whole time period with some transient oscillations at the step changes. It is shown also that the input current is directly proportional to the required output power.

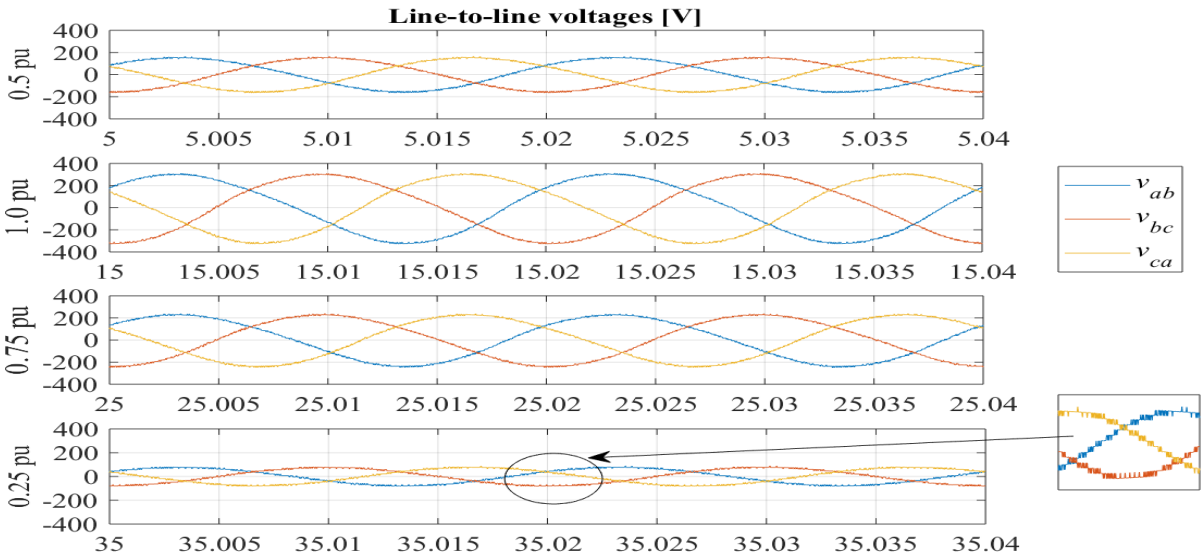

FIGURE 4.41: Line-to-line voltages

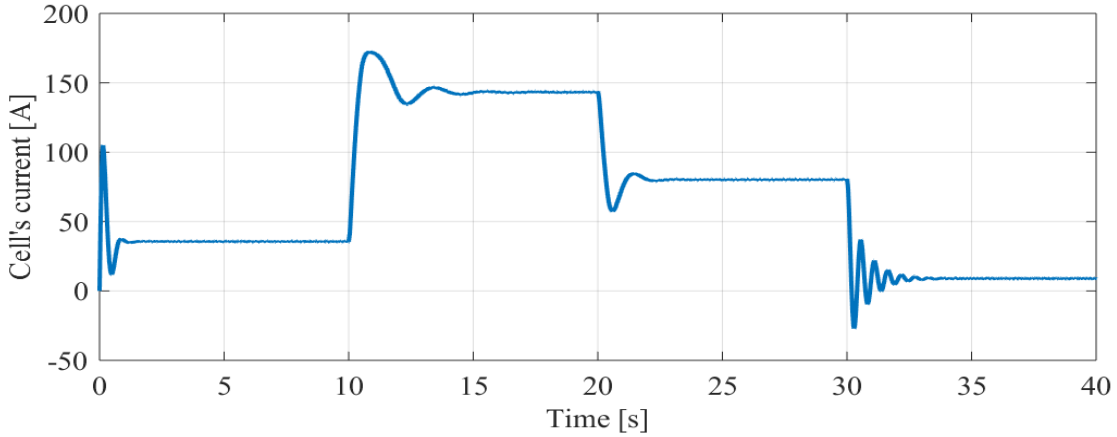

FIGURE 4.42: Battery cell's current

Chapter 5

Conclusions and Future Work

5.1 Conclusion

The proposed system introduced in this thesis provides a new cascaded single start multi-level converter, which is mainly based on connecting several sub-modules in series to form each phase (leg), where the core component is the bidirectional boost converter added in each sub-module, with no inverters and balancing management systems. The addition of the boost converter gives two main advantages to the SS-MMC; first, the small DC battery cell voltage is boosted to some higher value which helped in reducing the number of required SMs to get the needed output voltage. Second, it helps in having continuous input cell current and this increases the efficiency and the lifetime of the battery cells. CD-THIPWM modulation technique and voltage balancing algorithm were used to reduce the output ripple and THD. The proposed Converter is more reliable than conventional two-level inverters, and it has high efficiency. The system also can be used with v/f control even at low frequencies in order to control the speed of the motor.

And for sure, it is not empty of demerits; it is obligatory to leave the load ungrounded, and to employ WHY configuration only, in addition the need of using passive elements such as inductors, and super-capacitors, which may increase the cost and size of the converter. Simulation results yielded a relationship between the number of sub-modules and THD, in addition proved the predicted performance of the converter under v/f control. Simulation were carried out on static load under open loop and closed loop current control.

5.2 Future Work

The following outline is expected to be done in the future:

- Simulation of the converter under dynamic load with vector control, for flux and speed control purposes.
- Applying and simulate the proposed converter on a real existing EV.
- Practical prototype implementation for the lab testing.
- Designing appropriate snubber circuits for protection purposes.

Appendix A

MATLAB simulation models

A.1 Simulink Models for SS-MMC with No Load

A.1.1 Simulink Model with No Load

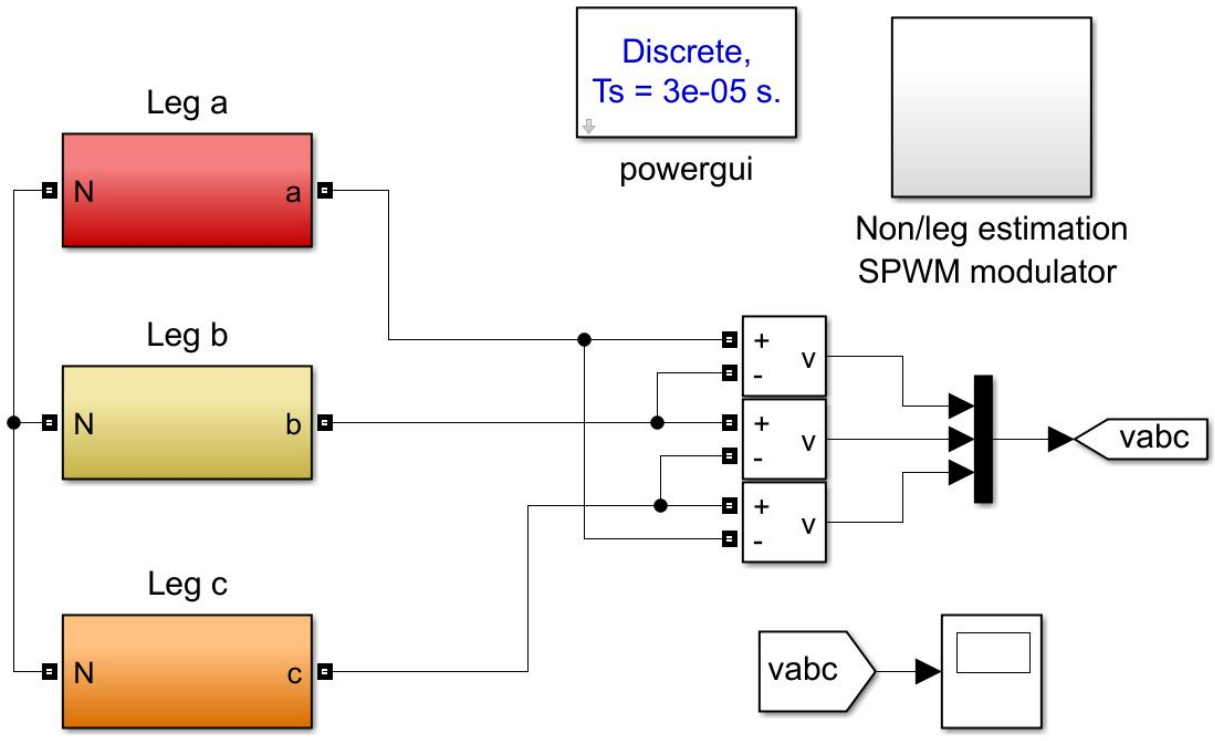

FIGURE A.1: SS-MMC Simulink model with no load

A.1.2 SS-MMC Leg-a Model

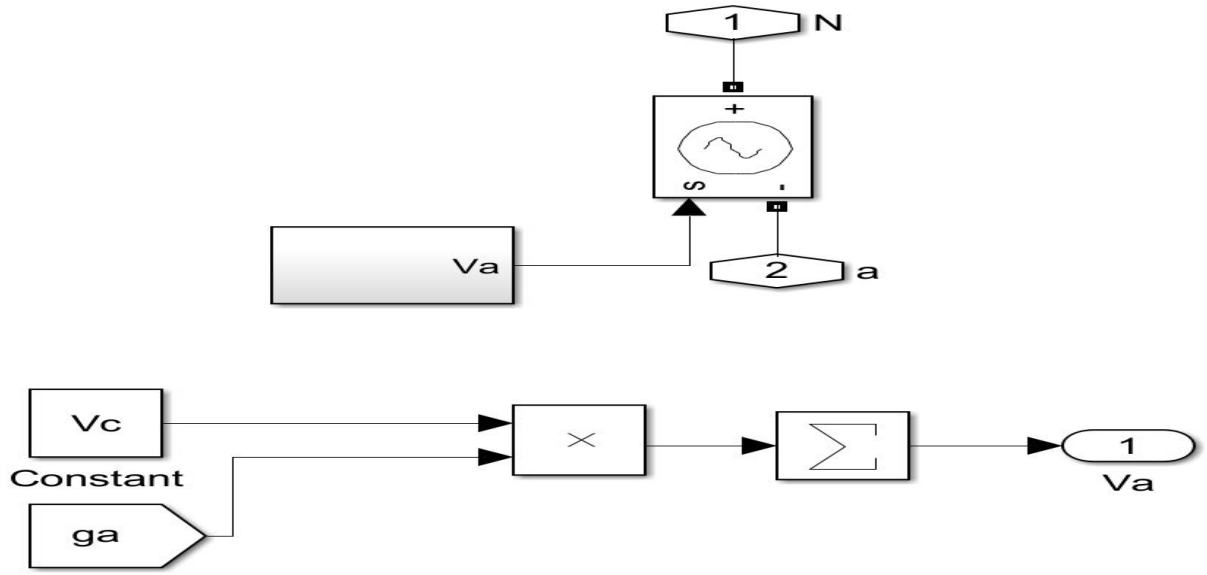

FIGURE A.2: SS-MMC Simulink leg-a model with no load

A.1.3 Modulation and Control Systems

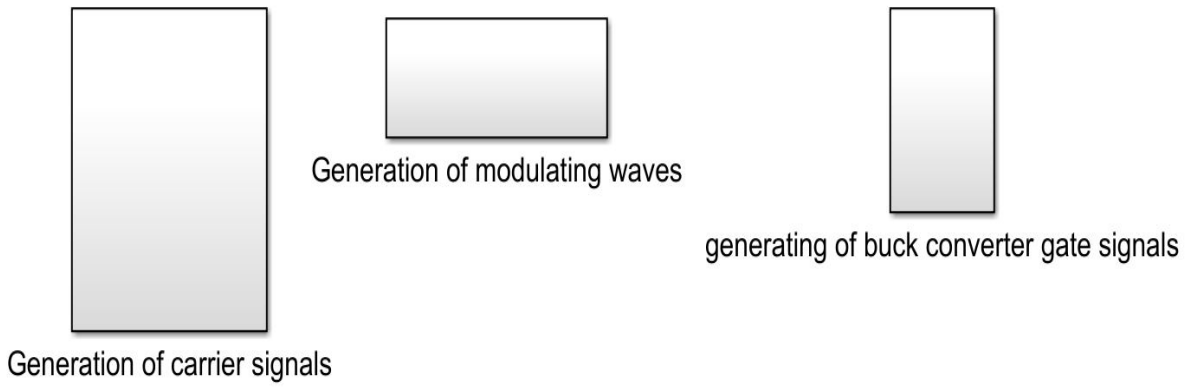

FIGURE A.3: Modulation and control systems blocks

A.1.4 Generation of Carrier Signals

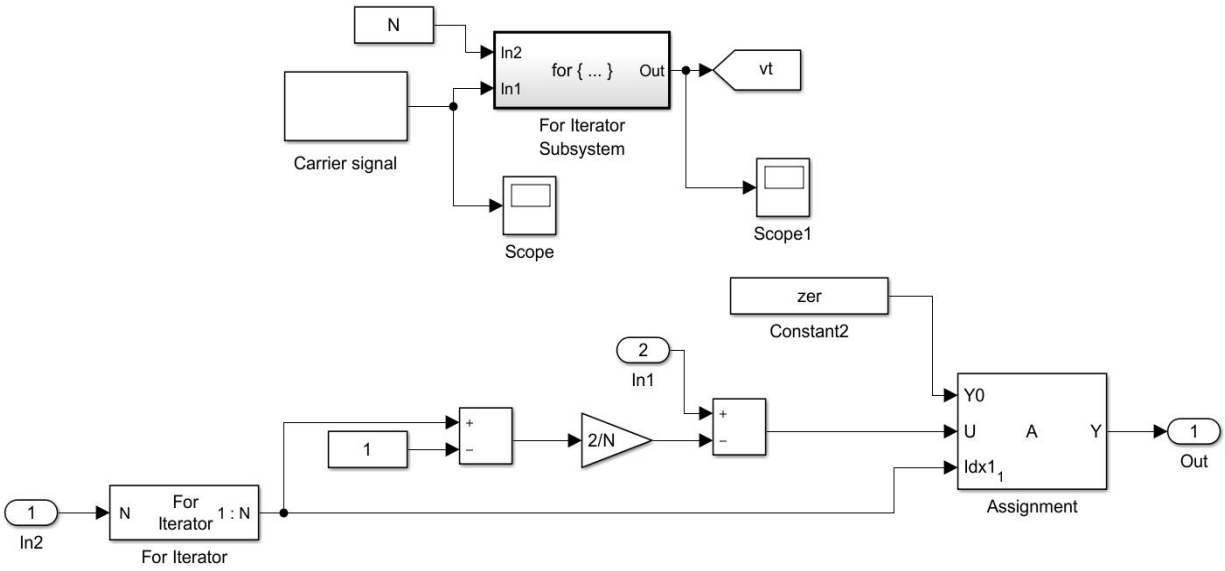

FIGURE A.4: Generation of carrier signals of SS-MMC with no load

A.1.5 Generation of Modulating Waves THI-SPWM

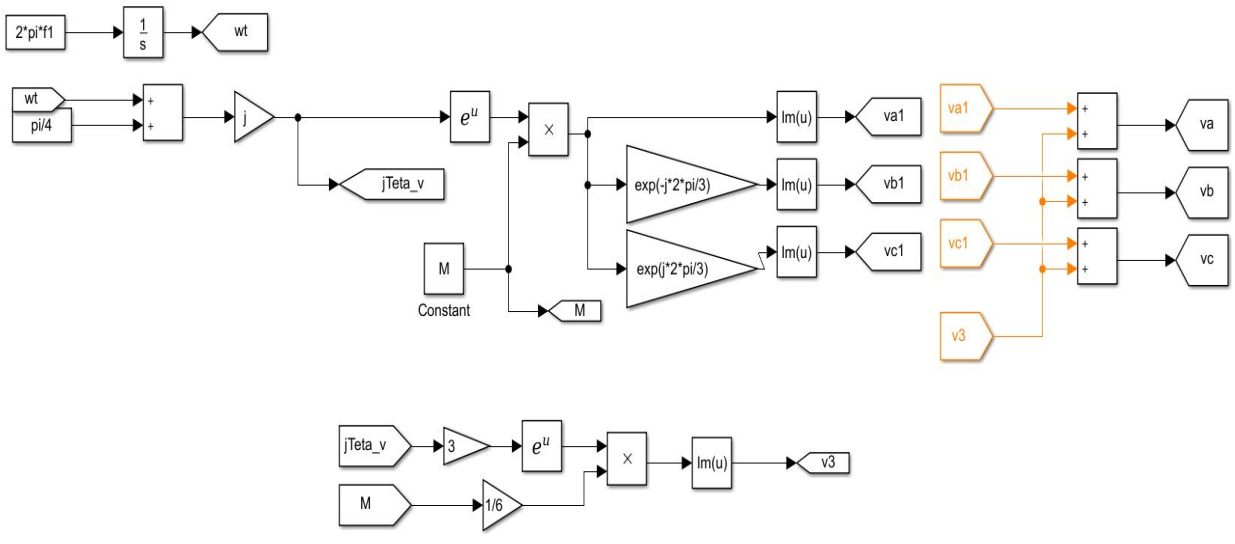

FIGURE A.5: Generation of modulating waves of SS-MMC with no load

A.1.6 Generation of Gate Signals for the Buck Converter

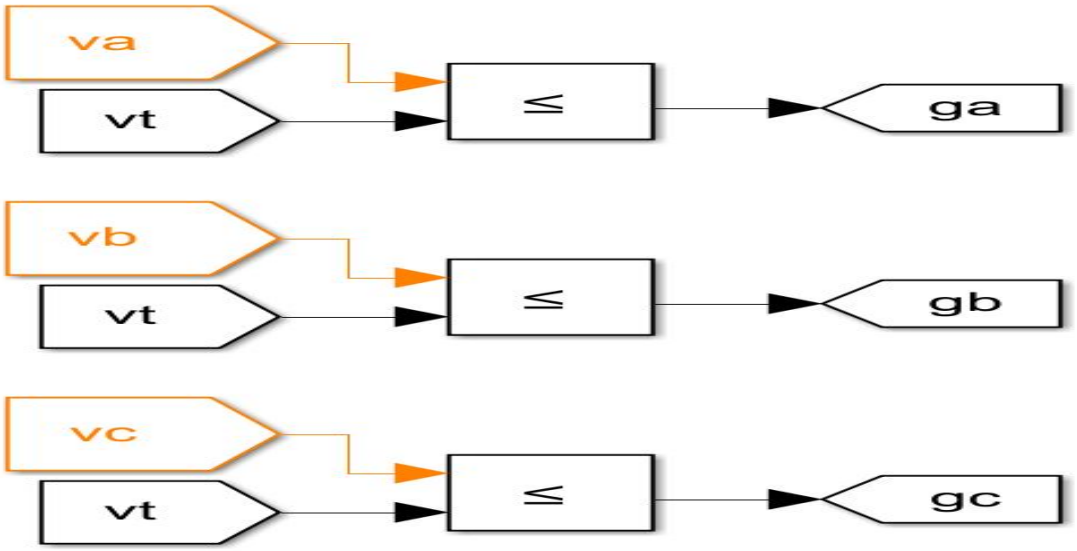

FIGURE A.6: Generation of gate signals for the buck of SS-MMC with no load

A.2 Simulink Models for SS-MMC with Static Load

A.2.1 Simulink Model with Static Load

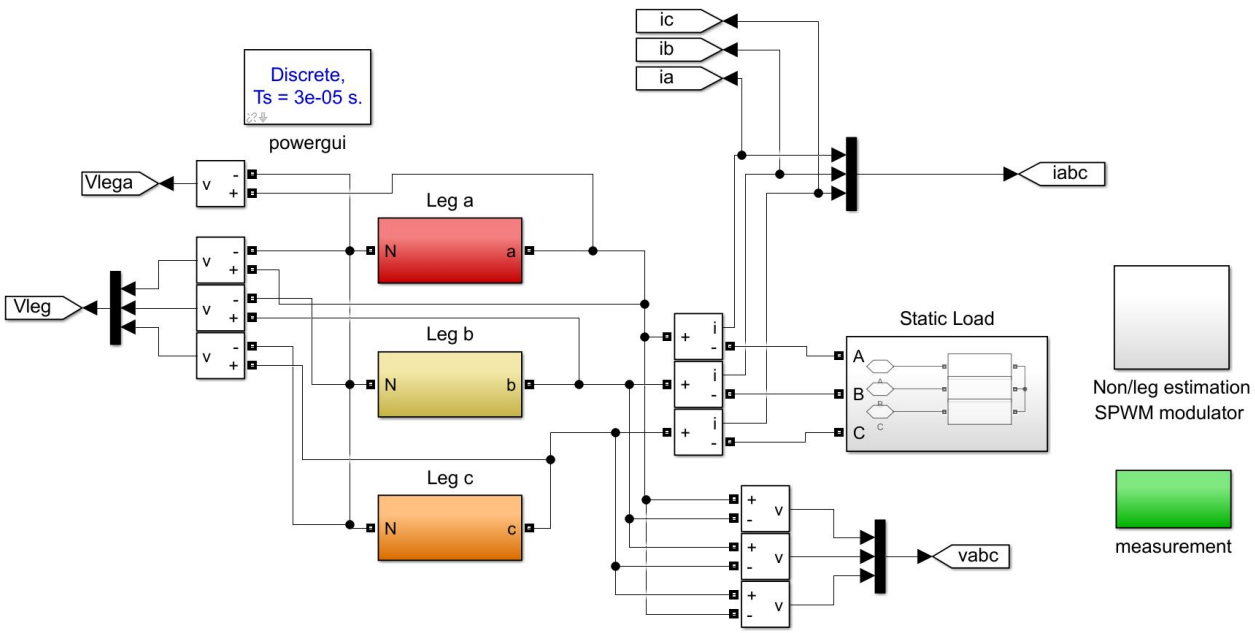

FIGURE A.7: SS-MMC Simulink model with static load

A.2.2 SS-MMC Leg-a Model

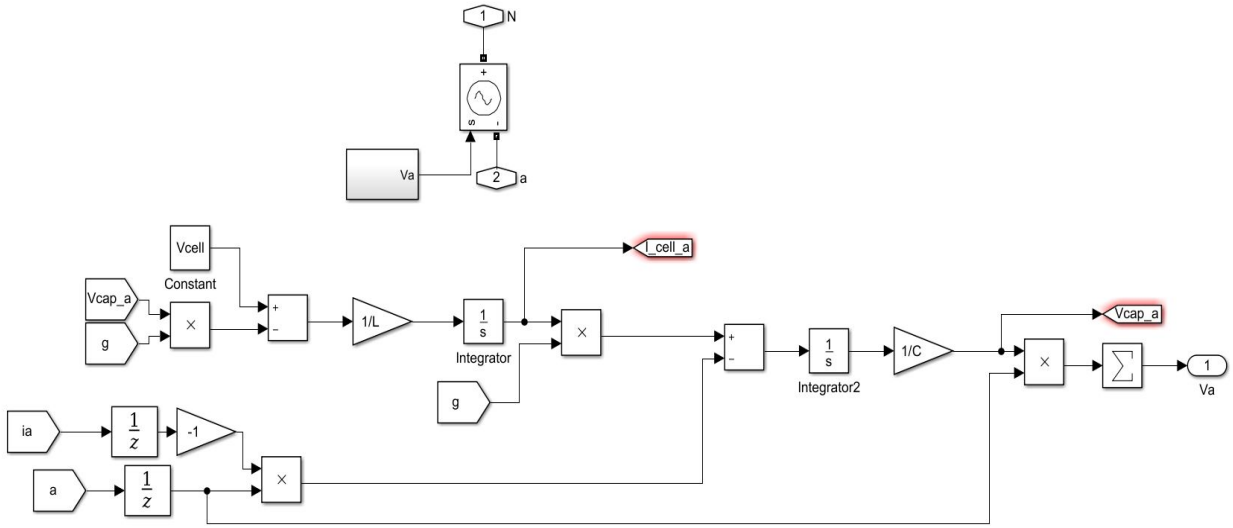

FIGURE A.8: SS-MMC Simulink leg-a model with static load

A.2.3 Modulation and Control Systems

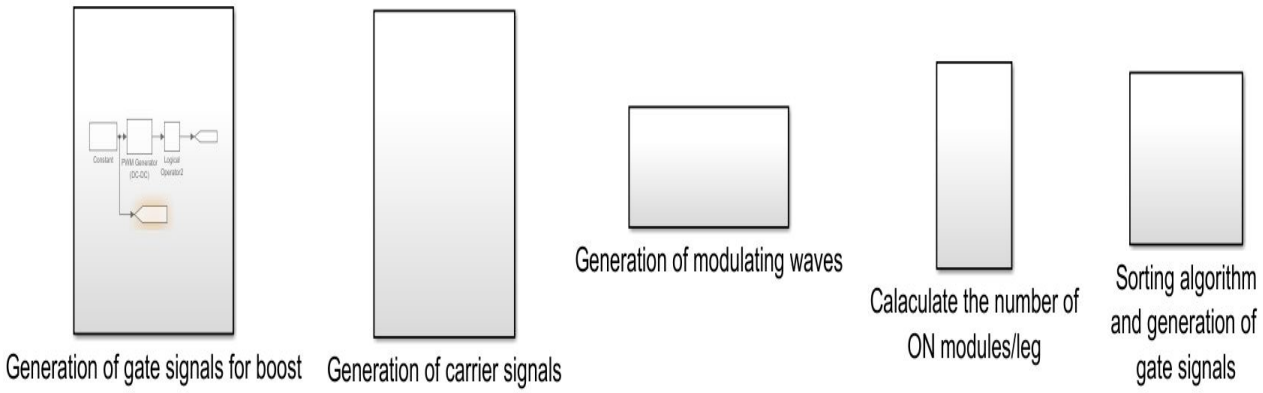

FIGURE A.9: Modulation and control systems blocks

A.2.4 PWM model for Bidirectional Boost Converters

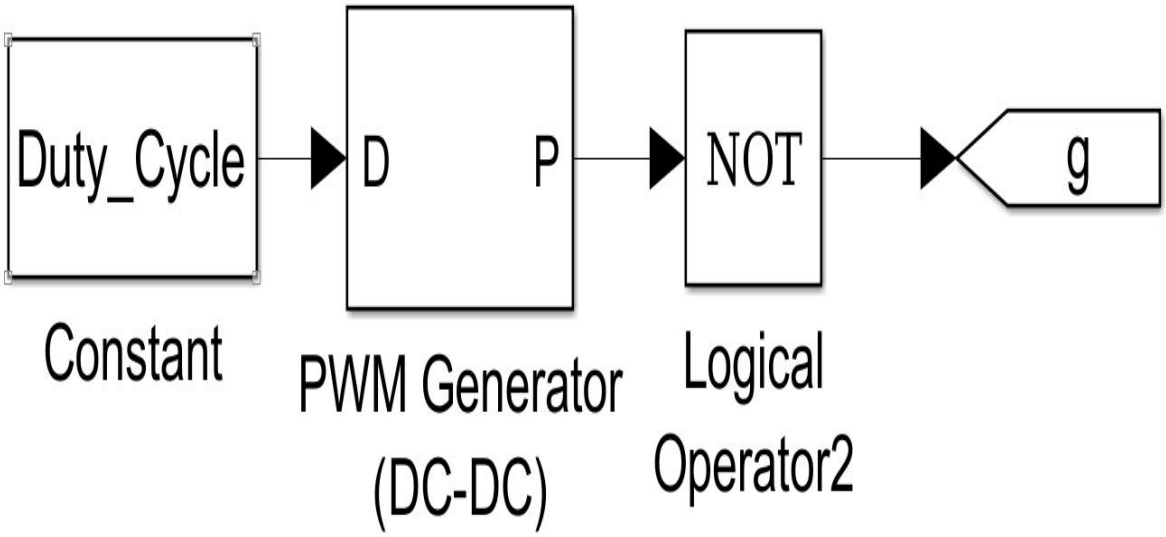

FIGURE A.10: Modulation and control systems blocks

A.2.5 Generation of Carrier Signals

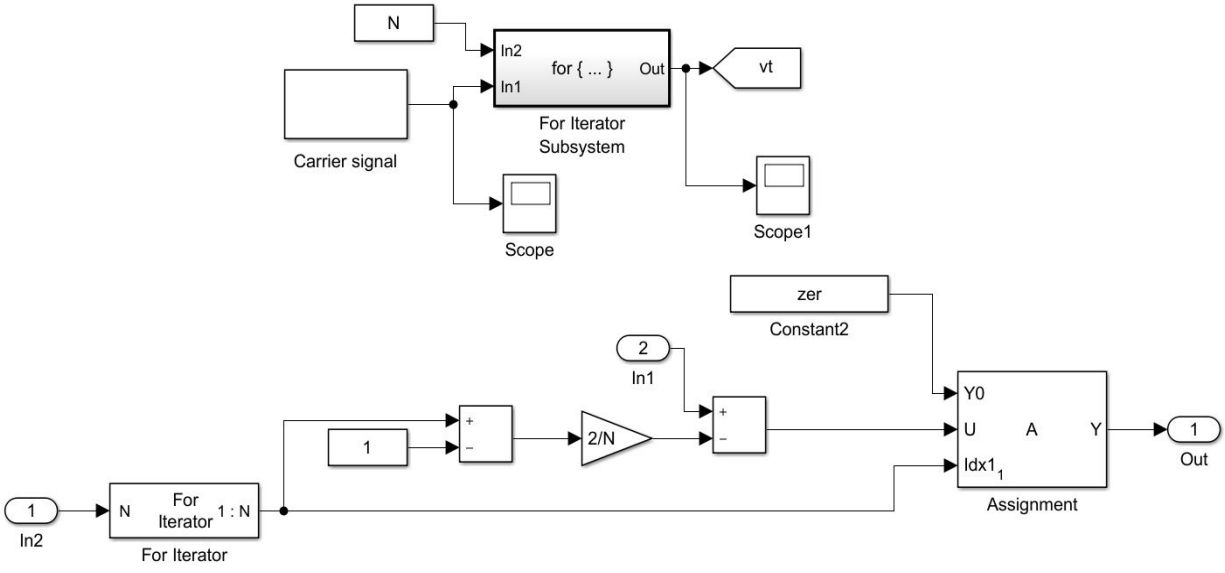

FIGURE A.11: Generation of carrier signals of SS-MMC with static load

A.2.6 Generation of Modulating Waves THI-SPWM

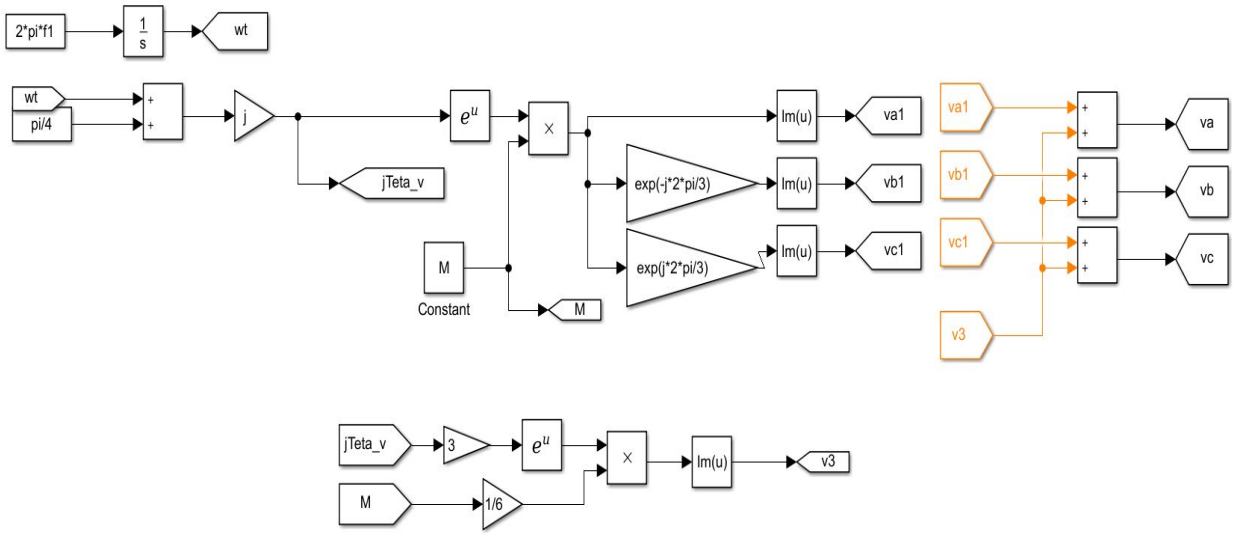

FIGURE A.12: Generation of modulating waves of SS-MMC with static load

A.2.7 Calculation of Active Sub-Modules

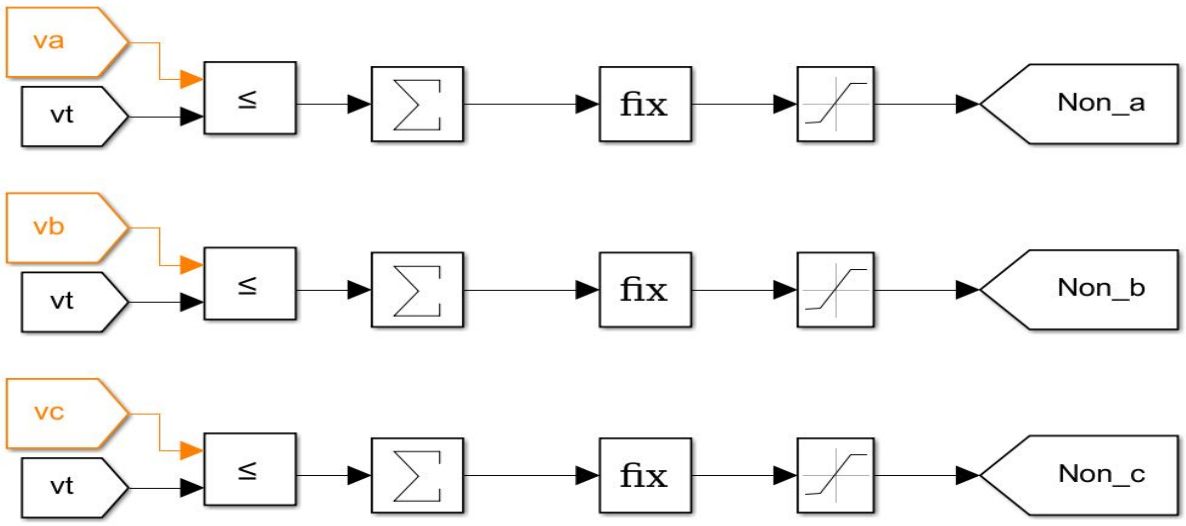

FIGURE A.13: Calculation of active SMs for SS-MMC with static load

A.2.8 Capacitor Voltage Balance Controller

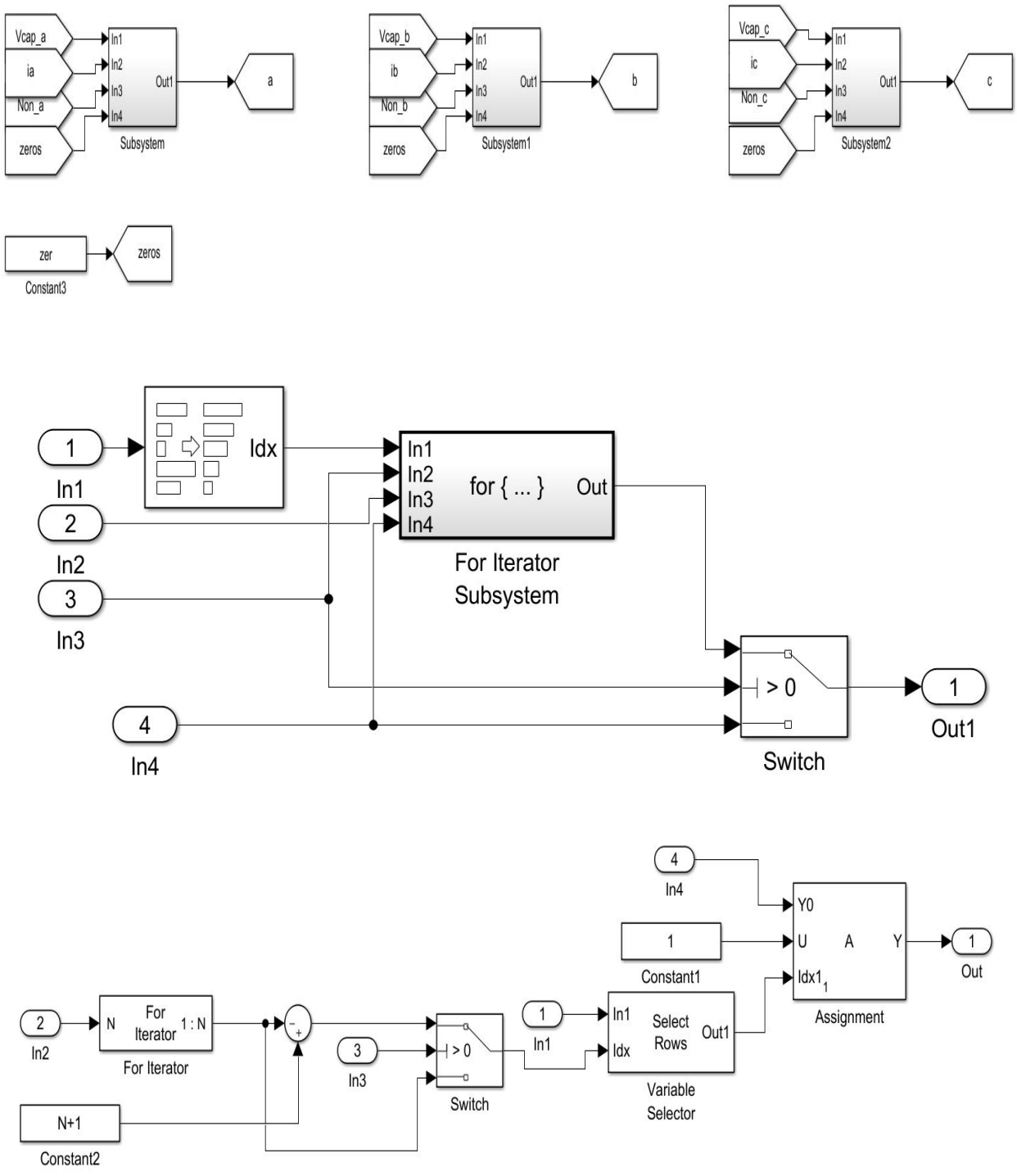

FIGURE A.14: Capacitor voltage balance controller for SS-MMC with static load

A.3 Simulink Models for SS-MMC with Static Load and current control

A.3.1 Simulink Model with Static Load and Current Control

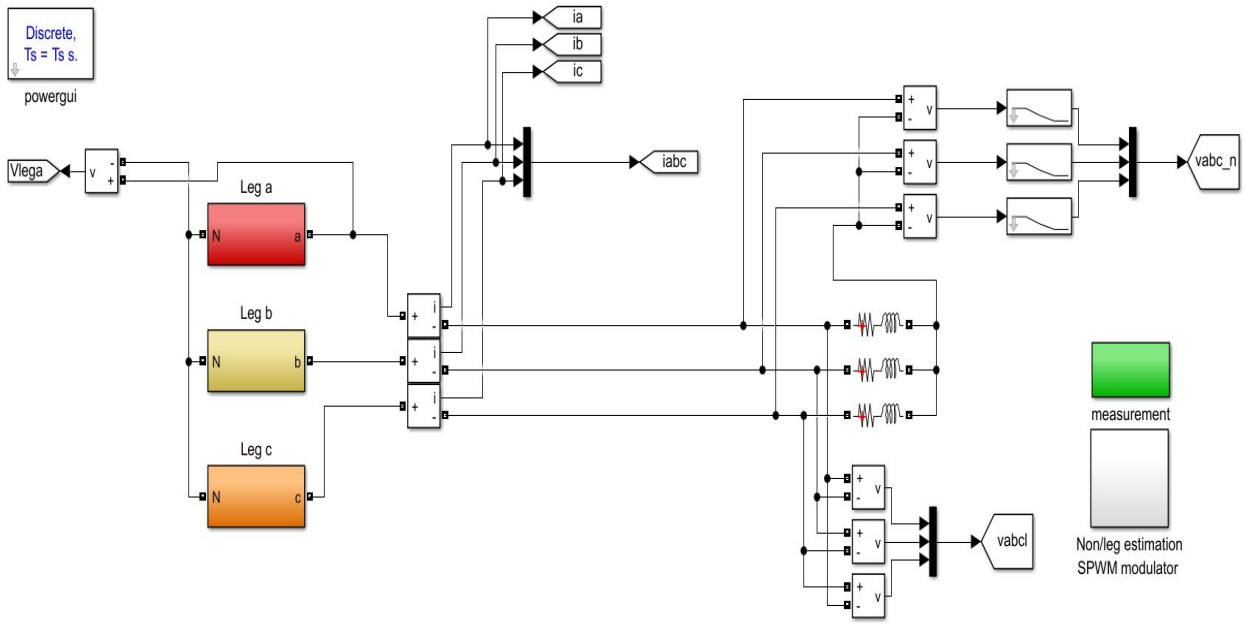

FIGURE A.15: SS-MMC Simulink model with static load and current control

A.3.2 SS-MMC Leg-a Model

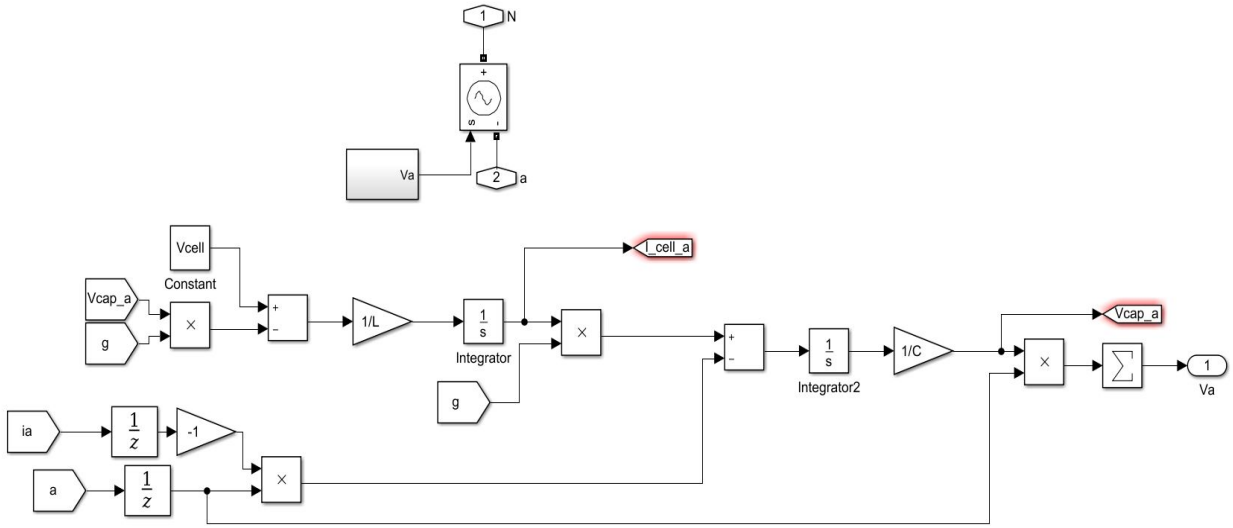

FIGURE A.16: SS-MMC Simulink leg-a model with static load and current control

A.3.3 Control Systems Blocks

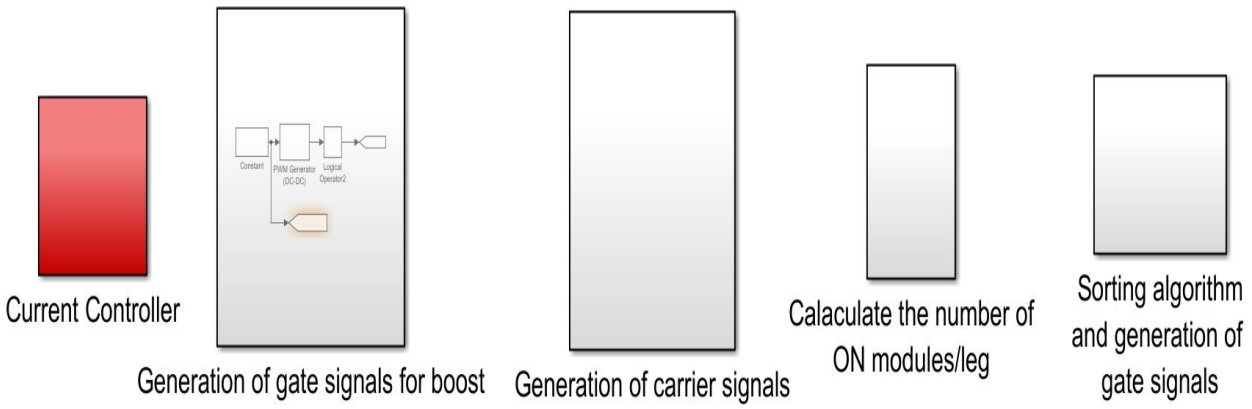

FIGURE A.17: Control systems blocks

A.3.4 PWM Model for Bidirectional Boost Converters

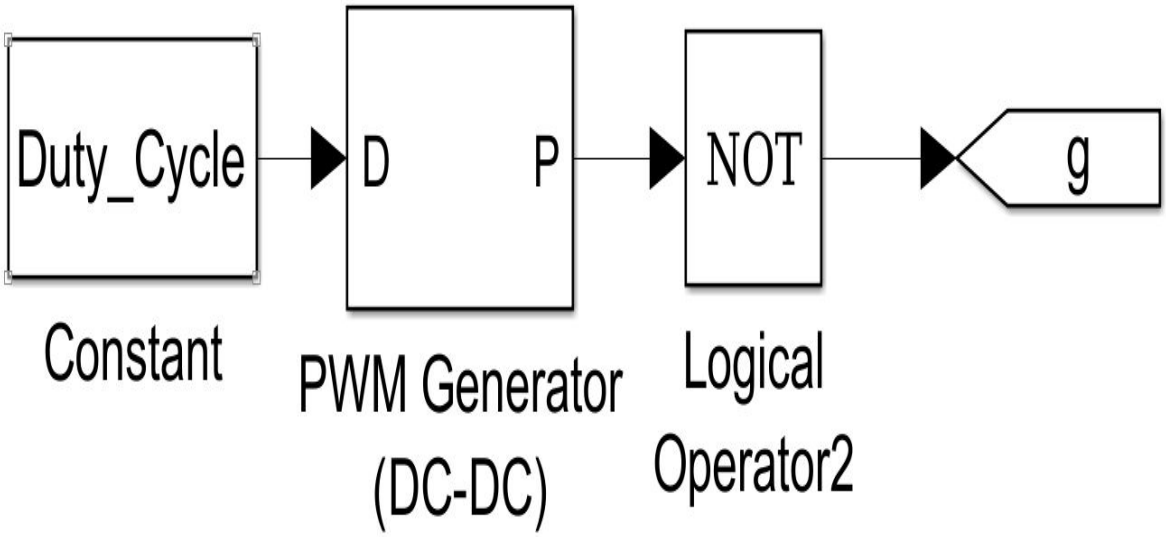

FIGURE A.18: Modulation and control systems blocks

A.3.5 Generation of Carrier Signals

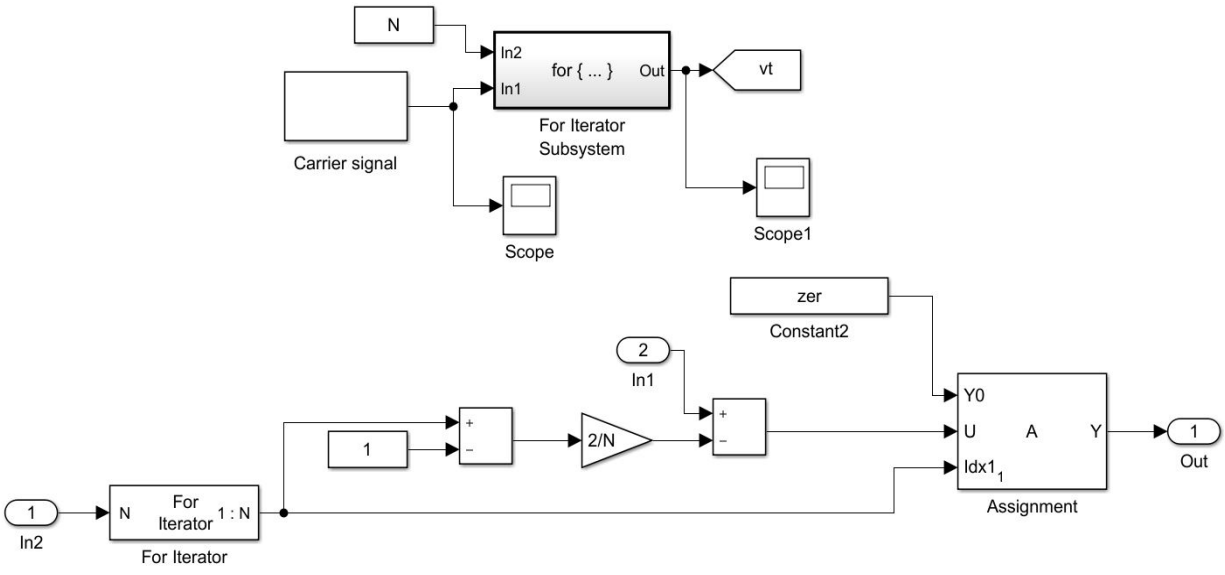

FIGURE A.19: Generation of carrier signals of SS-MMC with static load and current control

A.3.6 Current Controller Model

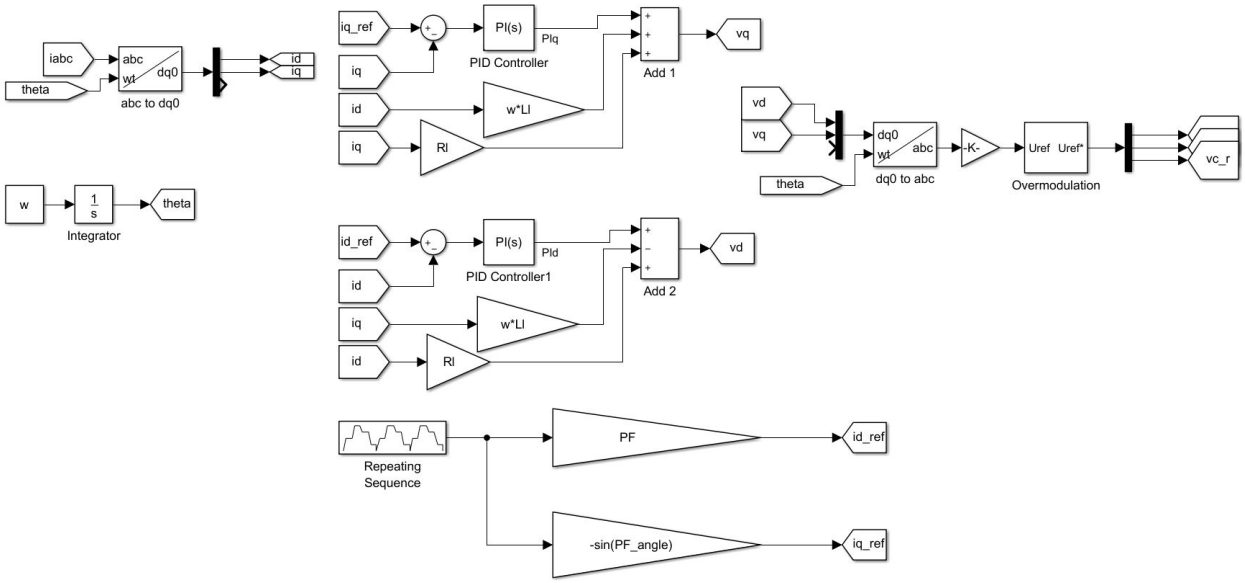

FIGURE A.20: Current controller blocks

A.3.7 Calculation of Active Sub-Modules

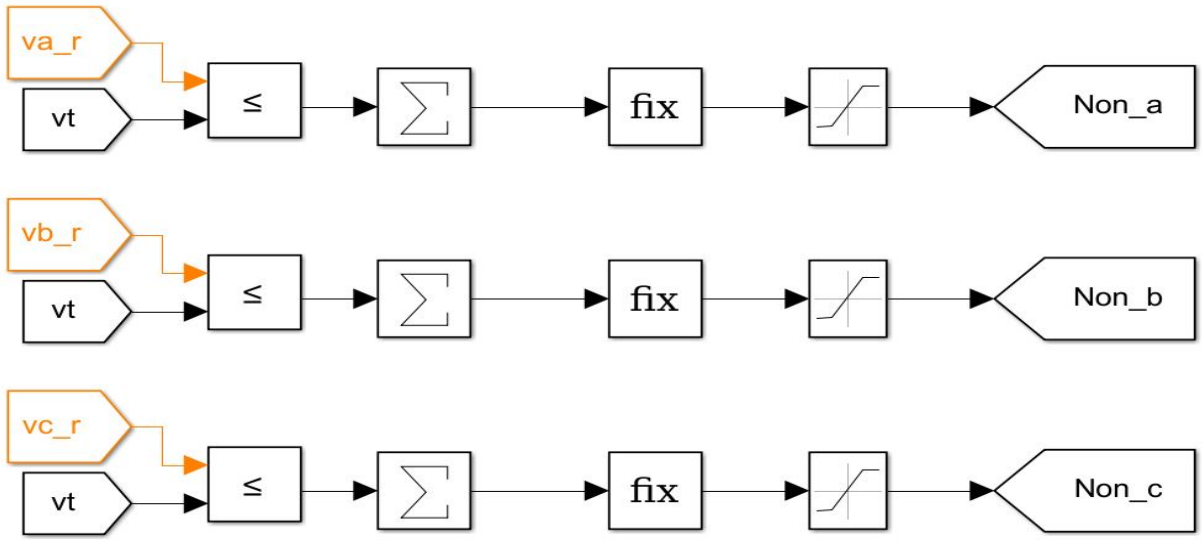

FIGURE A.21: Calculation of active SMs for SS-MMC with static load and current control

A.3.8 Capacitor Voltage Balance Controller

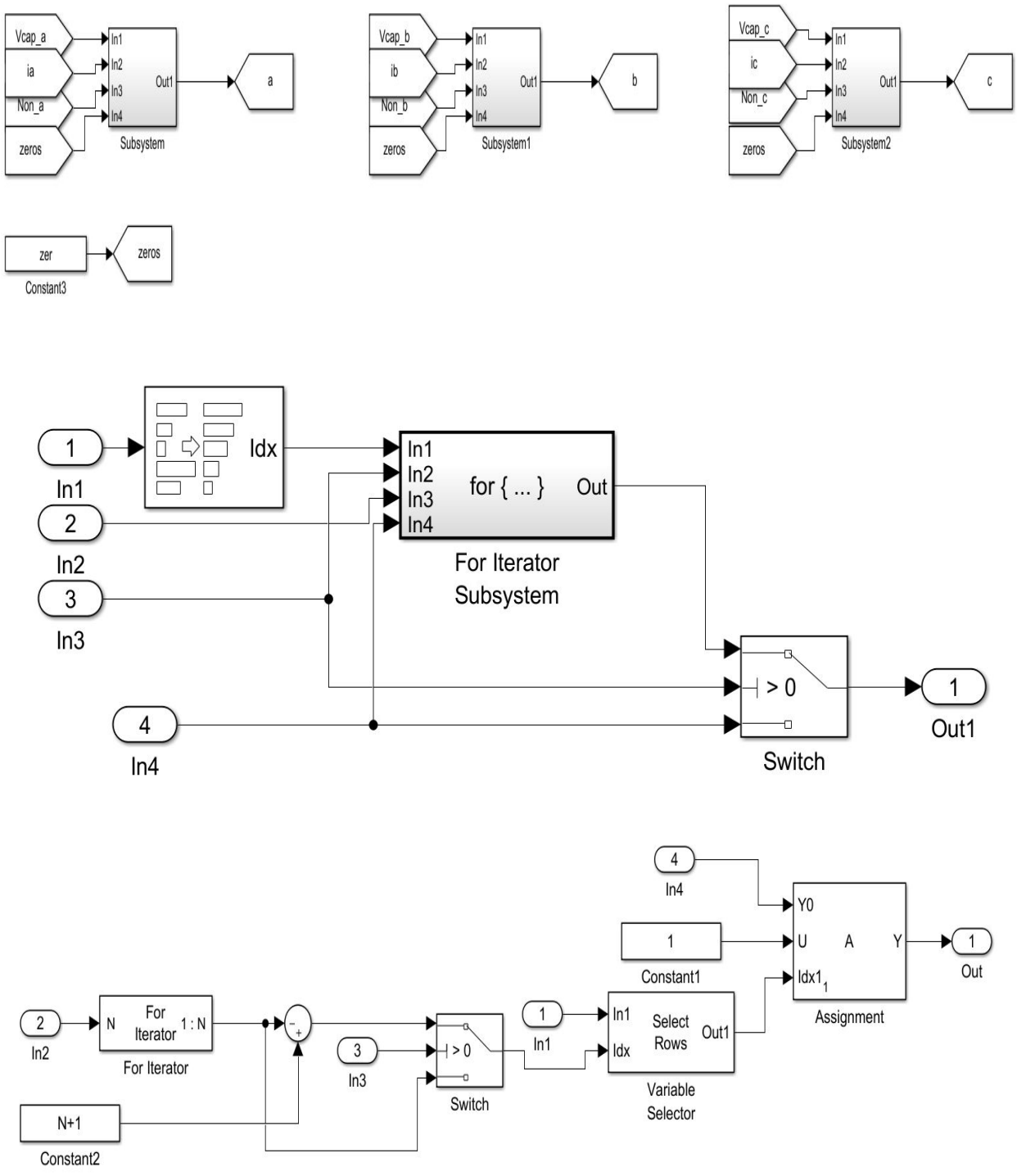

FIGURE A.22: Capacitor voltage balance controller for SS-MMC with static load and current control

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